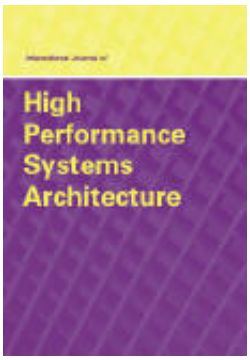

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High resolution digital pulse width modulator architecture using reversible synchronous sequential counter and synchronous phase-shifted circuit

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Abstract: Some of the advantages of the DC-DC converter digital control, such as programmability and improved control algorithms, have made it more popular in modern times. As a significant part of digital control, digital pulse width modulator (DPWM) is designed to fulfill number of requirements for high efficiency. The existing DPWM framework is implemented with high resolution along high switching frequency, but mandatory counter clock frequency is higher. To manipulate this drawback, the hybrid DPWM architecture is proposed that consolidates reversible synchronous sequential counter (RSSC) and synchronous phase-shifted circuit (SPS). The RSSC is employed to count trigger signal at each clock period. Whereas, SPS circuit is employed to select the clock by the quadrant phase-shifted clocks. The coding is activated in Verilog and the proposed RSSC design is synthesised utilising Xilinx ISE.

Keywords: DPWM; digital pulse width modulator; decoder; synchronous reversible counter; synchronous phase shifted circuit; reversible synchronous sequential counter; D-flip flop; delay line output duty cycle; linearity; time resolution.

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1 Introduction

Generally, digital pulse width modulator (DPWM) (Radhika et al., 2021; Rajesh et al., 2022) is used in electronic devices that are power management chips, LED drivers (Yu and Murari, 2021), base band signal processing etc. In DC-DC (Rao and Chakravarthi, 2020) converters are implemented using the DPWM with the advantages as insensitivity to process, voltage, temperature (PVT) variations (Papananos et al., 2020; Shajin et al., 2020), programmability advanced control algorithms, wide applicability while compare with the general analogue DC-DC converters. DPWM act as a converter for the signal of distinct duty cycle to analogue pulse width modulation that drives power transistors and it

produce high resolution (Cheng et al., 2020; Rajesh et al., 2022; Shajin et al., 2022), good linearity and low power consumption. High-resolution pulse-width modulator (HRPWM) is has high precision in the pulses edges and the resolutions exceeds the period of the system clock. Counter-based DPWMs are direct signals for analogue pulse width modulation, in which n-bit counter imitates triangular waveform that are likened to the digital code $K[n]$ for producing output signal (Alzaher and Alghamdi, 2020; Kipenskyi et al., 2020). Delay-line-based structures are used as the propagation delay in 2^n delay element (DE) linked in the cascade to produce the higher resolution pulse width modulation signal utilising 2^n input multiplexer including input signal $M[n]$ to select various delay cells outputs (Crovetti et al., 2020; Petric et al., 2021; Li et al., 2021; Shrivastava et al., 2020; Gharajeh and Haghparast, 2020)

In this manuscript, hybrid DPWM architecture is proposed which combines 4 blocks. Hybrid DPWMs are executed by incorporating reversible counter, synchronous phase-shift circuit, delay line and phase locked loop (PLL). Here, HDPWM is normally use this PLL to create 4 phase-shift clocks, then the time resolution is equivalent to delay among 2 nearby phase-shift clocks. By using the delay cells, the delay line base hybrid structure is designed. The hybrid structures give the counter clock frequency requirement as well as upgrade the time resolution, linearity. The cascaded DCMs have been utilised to DCM-base and delay line-base design to maximise the resolution. These 2 models not only minimise the linearity of digital PWM, but also maximise the delay of critical path along resource (area). These designs are affected through the trade-off between the linearity, time resolution, resolution, resource (area).

The major contributions of this manuscript are summarised as,

- The hybrid DPWM design is proposed which consolidates RSSC and phase-shifted circuit.
- The proposed design has 4 blocks, such as Decoder, synchronous reversible counter, Synchronous Phase-Shifted Circuit, and Delay line.
- The Reversible synchronous counter is employed to count trigger signal at each clock period.
- The SPS circuit is employed to choose the clock via quadrant phase-shifted clocks.
- For predicting the output, the circuits uses D-Flip flop to leave adequate slack amid the set and reset signals for eradicating glitch.
- The delay line is considered to set the DPWM time resolution.
- The coding is carried out in Verilog, then the proposed synchronous counter design is synthesised by Xilinx ISE.
- The performance metrics, viz path delay, output duty cycle (ODC), linearity, time resolution are examined.
- The efficiency of the proposed HRDPWM-RSSC-PSC is analysed with existing Hyb DPWM-SPSE-DL (Cheng et al., 2020), Hyb DPWM-DLP (Sun et al., 2020).

Remaining sections of this manuscript is delineated as: Section 2 portrays the recent studies, Section 3 illustrates about the proposed design, Section 4 proves the outcomes with discussion, Section 5 concludes this manuscript.

2 Literature survey

Among the frequent research work on DPWM; some of the latest investigations were assessed in this part,

Cheng et al. (2020) have presented the synchronous phase-shift circuit with delay line based higher resolution digital PWM. The critical path performance was analysed by the synchronous phase-shift circuit then the resolution of time was improved with the help of delay line depending on carry chain. Similarly, the combined process shows the hybrid DPWM. Finally it gives high linearity and the time resolution. This method was limited due to output variations.

Sun et al. (2020) have presented a delay-line DPWM with compensation module, delay-adjustable unit depends upon delay locked loop. While the duty cycle resolution was increased, digital pulse width modulations affected on its clock frequency, temperature as well as time error and it becomes larger. Delay-adjustable unit was depending on multiplexer, delay paths along various delay time, which frequently reduce the temperature or frequency via the input clock. Error was reduced using the time compensation technique by the critical path. Its temperature was high.

Morales et al. (2020) have presented a high-resolution all DPWM structure along tuneable delay element in CMOS. It was depending on digitally controlled delay element which was the combination of the uneven time interval up to 54 picoseconds, adjustable against PVT variations. The Hybrid DPWM allows for getting the duty cycle with 18-bit resolution and it could not use the internal clock with high frequency and the low power dissipation also maintained. HDPWM has improved performances, but it was limited due to delay.

Arora et al. (2021) have presented the Digital PWM utilising Direct Digital Synthesis. DPWM was digitally controlled power converters. It was cost effective, high performance as well as functionally integrated with small packaged-sized. Where, delay was increased.

Bhardwaj et al. (2020) have presented a FPGA-base higher resolution digital PWM utilising interleaving of phase-shifted clock pulses. The DPWM was utilised in switch mode power converts to make higher frequency pulses and to give the semiconductor switching circuit. DPWM was developed to generate the resolution of DPWM and the advanced FPGA clock management. The 13-bit digital PWM along 45 phase-shift clock pulses interleaving was carried out in Spartan3AN FPGA kit utilising 10 MHz

clock frequency for obtaining 12.5 ns the DPWM resolution, which was 8 times superior to that acquired by the simple counter-base model. The presented method consumes high power dissipation.

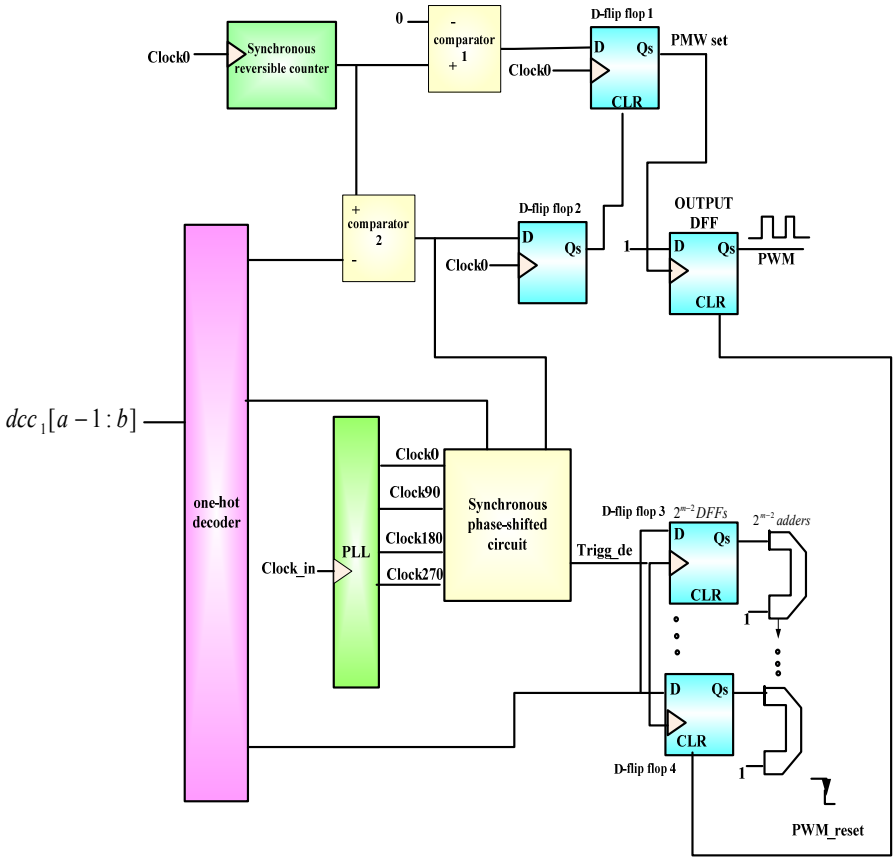
Nguyen et al. (2019) have presented the Phase-shift carrier pulse-width modulation along enhanced dynamic presentation for modular multiple level converters. The presented algorithm as well as capacitor voltage balancing control removes the tedious proportional-integral parameter tuning process requirement. It raises the dynamic performance estimated with conventional models. It consists of high modality, easy scalability. The presented method was limited due to low frequency.

Cheng et al. (2021) have presented the higher resolution hybrid DPWM (HRHDPWM) along dual-edge-trigger flip with hardware compensation. HRHDPWM was designed using the counter, phase shift circuit, carry chain. The presented dual-edge-triggered flip-flops were utilised to create the signals including 45° phase shift in the phase-shifted circuit and the hardware compensation was used to maximise the duty cycle which affect the regulation accuracy of the converters. It was used to reduce the resource compensation but it was consumes high power.

3 Proposed methodology

In this, the DPWM architecture is designed and it is given in Figure 1. It includes decoder, proposed reversible synchronous counter, phase-shifted block, delay line and D flip-flop. Here, the input duty cycle command is denoted as $dcc\left[a-1:0\right]$, input clock for PLL is denoted as CLK_in and the output signal of DPWM is denoted as $Output_{DPWM}$. The detail description about each blocks used in DPWM is given below.

Figure 1 Proposed design of high resolution digital pulse width modulator architecture (see online version for colours)



3.1 Decoder

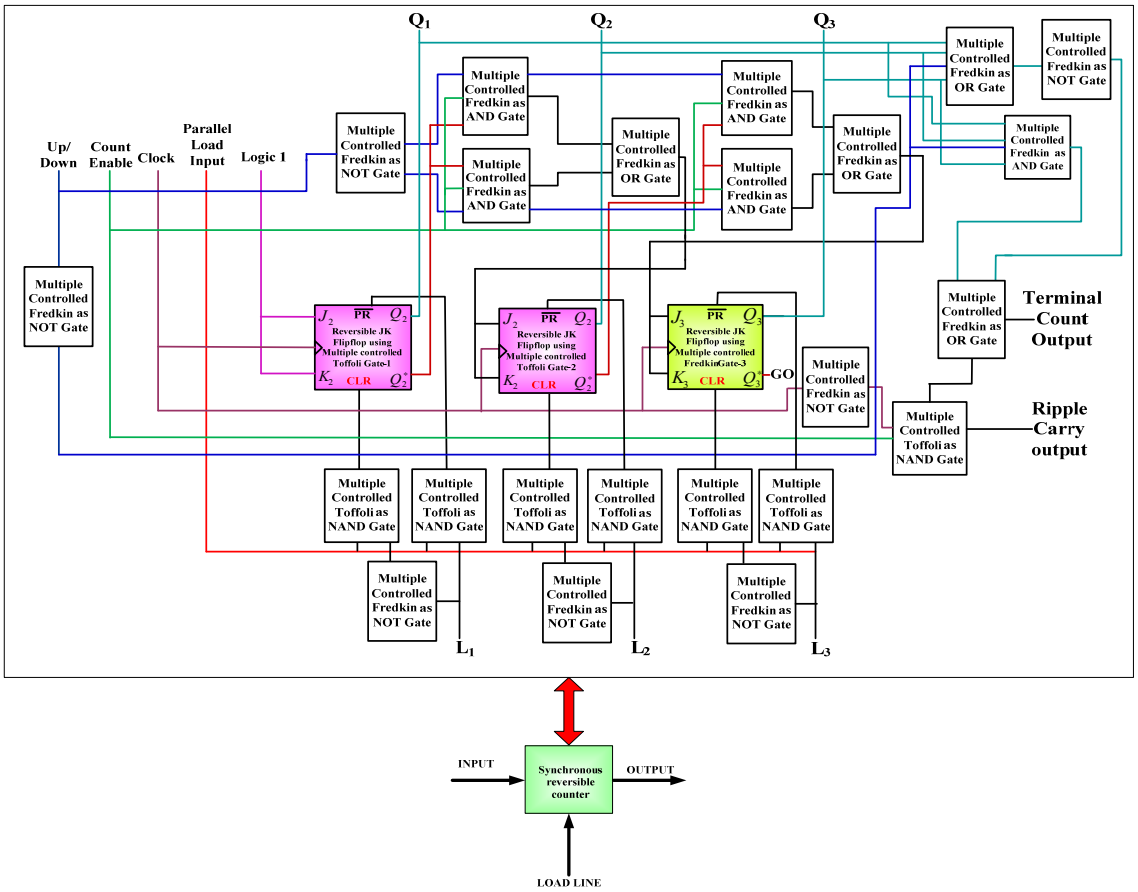
The purpose of decoder is to separate the command of input duty cycle $\{dcc\left[a-1:0\right]\}$ as $dcc_1\left[a-1:b\right]$, $dcc_2\left[b-1:b-2\right]$ and $dcc_3\left[b-3:0\right]$. Here dcc is represented as the input duty cycle, $a\,b$ most and least significant bits, $dcc_1\left[a-1:b\right]$ denotes input duty cycle command most significant bits, $dcc_2\left[b-1:b-2\right]$ denotes input duty cycle command secondary significant bits, $dcc_3\left[b-3:0\right]$ and denotes input duty cycle command least significant bits.

3.1.1 Reversible synchronous sequential counter

In high resolution DPWM, the reversible synchronous sequential counter (RSSC) is proposed. The reversible logic is used because of its low power consumption and less delay. Here the reversible synchronous counters are

designed using Multiple Controlled Toffoli (MCT) as well as Multiple Controlled Fredkin (MCF) reversible logic gates using 3- JK flip flops. JK_1 and JK_2 flip flop is designed using the MCT. Similarly, JK_3 flip flop is implemented using the MCF gate. Basically the MCT gate does the following gate functions, such as NOT, AND, NAND, XOR. For JK_3 flip flop, MCF gate is used. The reversible MCF gate does the following gate functions such as NOT, AND, OR, NOR. By this delay is reduced, power consumption is low and the speed is increased in Proposed Reversible Synchronous Counter with Multiple Inputs and Outputs. Figure 2 shows the Synchronous reversible counter design using MCT and MCF reversible logic gates.

Figure 2 Synchronous reversible counter design using MCT and MCF reversible logic gates (see online version for colours)



The synchronous counter block is utilised to set PWM_SET signal for getting the D-flip-flop output as well as trigger signal $Trigger\_signal$ to the reversible synchronous phase shift circuit. At Figure 1, PWM_SET is produced while the output of counter is same as 0. At this time, the output of the comparator is compared with the decoder 1 $dcc_1[a-1:b]$ with the comparator-2. If the counter is equal to $dcc_1[a-1:b]$, trigger signal ($Trigger\_signal$) is in active state. After that the 2D-flipflops are provides as the synchronous process. In this P_S is represented as the relationship among the switching period, $CP_{counter}$ is represented as the clock period of the counter and its equation is given in equation (1)

$$P_S = 2^{a-b}.CP_{counter} \quad (1)$$

3.1.2 Synchronous phase- shifted circuit

This circuit is selected the clock via the quadrant phase-shifted clocks. In the previous synchronous phase shift circuit 4:1 MUX is used, it cause unexpected nonlinearity problem, so that the MUX block is replaced with the D-flip flops. It consists of on-chip PLL, 4 D-Flip flop, 4 AND gate and 1 OR gate. The PLL is used to generate four quadrant phase-shifted clocks, such as *Clock*0, *Clock*90, *Clock*180, *Clock*270 with 50% duty cycle. In this *Clock*0represented as the counters clock signal of positive edge generator. In this 4 D-flip-flops are used and its clock inputs/signals are taken from the four phase-shifted clocks. From this the first D-flip flop 1 takes the *Trigger_signal* from the positive edges of the *Clock*1 for generating the trigger signal-1 that is

*Trigger*_1. Similarly, D-flip flop 2, D-flip flop 3, D-flip flop 4 generates the Trigger signal 1, 2, 3, 4 that is *Trigger*_1, *Trigger*_2, *Trigger*_3, *Trigger*_4. While transmitting the trigger signal to the D- flip flops and it generate the trigger signal as $Trigger\_n(n=1\approx 4)$, (n is represented as the number of trigger signals) only on phase shifted clocks positive edges. In this, $Trigger\_n(n=1\approx 4)$ is known as the optimum phase-shift clocks that synchronised the phase-shift clock propagation path and trigger signal. While using D flip flop, the clock delay problem is reduced, because the D-flip flops wait till the positive edge of related phase-shift clock reaches for capturing the prior DFF output. And trigger signal $Trigger\_n(n=1\approx 4)$ problem also reduced, while crossing the two adjacent DPWM switching periods, therefore the D-Flip flops 1, D-Flip flops 2, D-Flip flops 3, D-Flip flops 4, are reset by $Clock\,90$ and $clock\,180$, $Clock\,180$ and $clock\,270$, $Clock\,270$ and $clock\,0$ and $Clock\,0$ and $clock\,90$ respectively. After replacing MUX, the synchronous phase shift circuit utilises 4 two-input AND gates together with 1 four-input OR gate. To assure these gate locations are set in location allocations, the restriction for global signal on every path is needed, thus creating every path equivalent delay. The 4 AND gates outputs are injected into 4-input OR gate. By then, Synchronous Phase- Shifted Circuit is designed for DPWM design.

3.1.3 Delay line

This is set the time resolution of digital PWM. The propagation delay of carry bit in every added is constant then it is able to predict the values from 10-100ps. Similarly, to check the linearity, the carry chain total delay is equivalent to delay among the 2 adjacent phase shifted clock (D_{CPS}). The carry chain uses 2^{b-2}adders and its equation is given in equation (2)

$$D_{CPS} = 2^{b-2}.D_c \tag{2}$$

where D_c represents carry delay of the adder, CPS implies carry pulse signal, D implies delay line. The high resolution digital PWM is recognised by maximising the bits count of counter, the count of cascaded phase-shifted circuits, or delay line length. This architecture can reach the 18-bit maximal resolution, while managing better performance of linearity with time resolution. The generalised design process of the proposed approach is delineated below. To activate n-bit digital PWM with necessary time resolution D_c the parameter a should be designed firstly. D_c is structured to compromise resource (area) and power, since large a means more adders, thus large area of carry chain, according to equation (2), $CP_{counter} = 2^{b-2} \cdot D_c$ from equation (3), smaller a means smaller $CP_{counter}$, named high frequency of counter along high power. Figure 1 contains Reversible synchronous counter, delay line, synchronous phase-shifted circuit (SPS) and resolution of this circuit is given as a and it is represented as the number of bits. Thus, higher resolution DPWM is recognised by maximising the bits count of counter, count of cascaded phase-shifted circuits, or delay line length. When maintaining better presentation of linearity with time resolution, it reaches greatest 18-bit resolution.

With the help of RSSC, the SPS, delay line, and the resolution of this circuit is given as a and it is represented as the number of bits parameters the high resolution DPWM is designed. To design the high resolution DPWM with the needed time resolution D_c, first design parameter a. In this, a is designed for compromising resource (area) and power. If the power is increased more number of adders are included. For reducing the power and area less number of adders are used according to the equation (2) therefore the use of counter is also lowered. Therefore, the counter's clock period $(CP)$is given in equation (3)

$$CP_{counter} = 2^{b-2} \cdot D_c \tag{3}$$

The switching period of DPWM is given in equation (1) that is $P_S = 2^{a-b}.CP_{counter}$. This block output denotes PWM_Reset and it represents reset signal of output D-Flip flop. By this process, the negative edge of the DPWM pulse is generated.

3.1.4 Output of D-Flip flop

D-Flip flop is employed to cause adequate slack amid the set and reset signal and to avert glitch. It attains maximal resolution of linearity and time resolution. While using RS latch, the slack is not able to predict, delay is non-negligible, and not able to calculate the time. So, the DPWM with RS latch does not create small pulse width that restricts range of duty cycle. So, the proposed architecture D-Flip flop is used for predicting the output instead of RS latch. The output is predicted in the D flip flop, where set as each time of PWM_Set and reset positive edge at the same time, when PWM_Reset in delay line is produced. By this process, the slack among the signal of set and reset requires to fulfil the set time as well as DFF hold time that is small duty cycle has permitted to attain. The carry delay of every adder is simulated to be 34ps in fast corner and 73ps in slow-corner, which is the time resolution of proposed carry chain and HRDPWM. It is clear that the carry delay is mostly unaffected by changes in PVT, which improves the dependability of digital controlled systems. Given that there is only one DFF and one adder in each building block, their locations correspond one by one, and the interconnection among DFF and adder within a same building block is extremely stable, thus ensuring the linearity of the delay line. Therefore the delay and the power is reduced in the proposed design.

4 Result and discussion

In this section, hybrid DPWM is proposed that consolidates RSSC and SPS circuit is discussed. The experimental outcomes acquired from external clock of 50 MHz internally multiply to 188 MHz by PLL, that is 188 MHz counter clock frequency. The overall 290 LEs are considered, the resource utilisation is 5%. The performance metrics is examined to examine the performance of the proposed method. The performance is analysed with existing high resolution digital PWM on the basis of SPS with delay line (HybDPWM-SPSE-DL) Delay-Line digital PWM including Compensation Module along Delay-Adjustable Unit based upon Delay Line (Hyb DPWM-DLP).

Figure 3 shows the Timing diagram of proposed HRDPWM-RSSC-PSC. From Figure 3 D_c represents carry delay of the adder, *CPS* is represented as the carry pulse signal, *CP* is represented as the counter's clock period, CLK is represented as the clock period, *Trig _CPS* is represented as the phase shift clock, *Trig _de* denotes delay line. Since $dcc1[13:7] = 0000101$, *Trig _CPS* is produced while Counter is equivalent to 5 (the decimal value related to 0000101). To $dcc1[6:5] = 11$, CLK270 is selected and *Trig _de* is produced with delay of $3 \cdot D_{CPS}$ 3

At last, $dcc1[4:0] = 11000$ is decoded then the overall delay of delay line is $24 \cdot D_c$. Once *Trig _de* reaches, this delay reset the output DFF and superimpose in pulse width modulation. The above 3 delays represent the on-time of pulse width modulation, and the ODC (PWM_{ODC}).

Figure 3 Timing diagram of proposed HRDPWM-RSSC-PSC

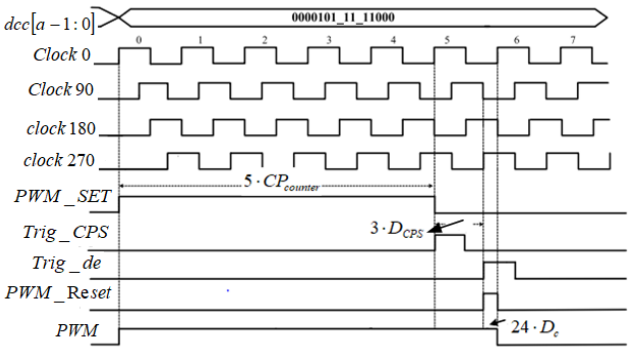


Figure 4 shows the Pulse signals for various decoders. Figure 5 displays the range of duty cycle for proposed HRDPWM-RSSC-PSC covers 0.9429% to 99.2% closer to 0-1 and the detailed experimental values are given in Table 1.

Figure 4 Pulse signals for various decoders for proposed HRDPWM-RSSC-PSC (see online version for colours)

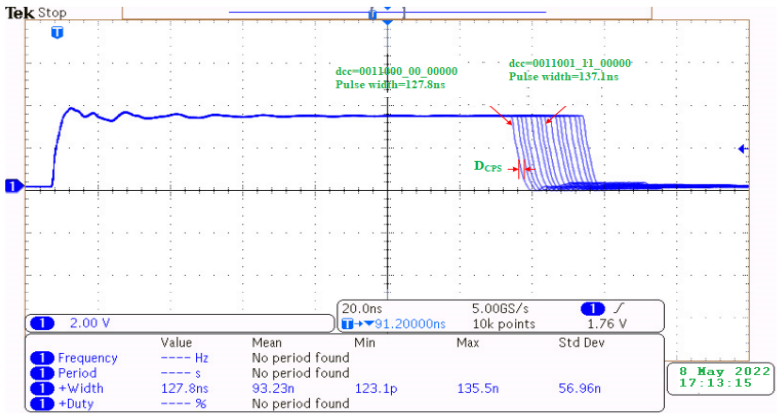


Figure 5 The range of duty cycle for proposed HRDPWM-RSSC-PSC covers 0.9429% to 99.2% closer to 0–1 (see online version for colours)

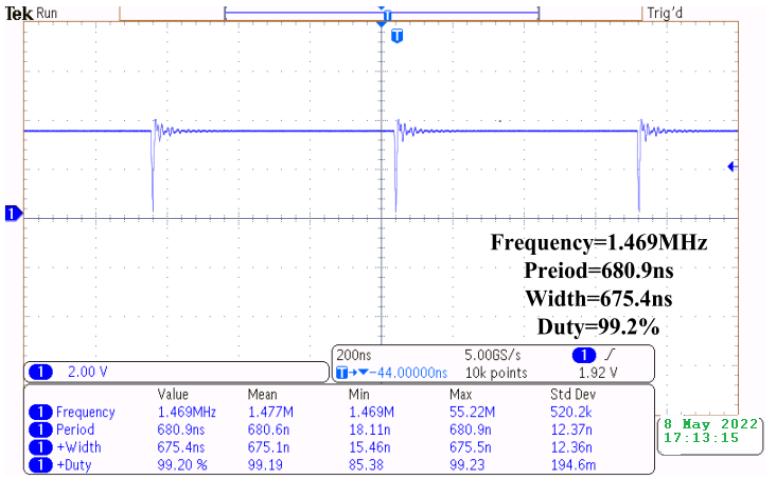


Table 1 Performance analysis

Performance metrics	*Hyb DPWM-SPSE-DL*	*Hyb DPWM-DLP*	*HRDPWM-RSSC-PSC* (*Proposed*)
Path Delay	1.017	0.97	0.323
Area(mm^2)	0.077	0.059	0.0073
Output Duty Cycle	0.78	0.76	0.99
Time Resolution (ps)	600	90	40.1
Pulse width	115	120	136
Power (mW)	20.94	29.45	0.213

Table 1 shows the performance analysis of path delay, area, ODC, time resolution, pulse width, power, frequency.

The performance of path delay of the existing designs, such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP are ineffectual to design synchronous counter with lesser path delay. The existing Hyb DPWM-SPSE-DL attains moderate performance of path delay than existing HRDPWM-RSSC-PSC design. For example, the existing Hyb DPWM-SPSE-DL attains maximal path delay 1.017, existing Hyb DPWM-DLP 0.97 lesser path delay value. But, the proposed HRDPWM-RSSC-PSC attains better outcome with 0.323 lesser path delay value. The proposed HRDPWM-RSSC-PSC design provides 53.09%, 34.86% lower path delay compared with existing designs, like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

The performance of Area of the existing designs, such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP are ineffectual to design synchronous counter with lesser Area. The existing Hyb DPWM-SPSE-DL attains moderate performance of Area over existing Hyb DPWM-DLP. If how it is, the proposed HRDPWM-RSSC-PSC outperforms existing design by attaining lesser Area. For example, the existing Hyb DPWM-SPSE-DL attains maximal Area 0.077, existing Hyb DPWM-DLP attains 0.059 slightly lesser Area value. But, the proposed HRDPWM-RSSC-PSC attains better outcome with 0.0073 lesser Area value. The proposed HRDPWM-RSSC-PSC design provides 13.82%, 25.93% lesser Area estimated with existing Hyb DPWM-SPSE-DL, Hyb DPWM-DLP designs.

The performance of ODC of the existing designs, such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP are ineffectual to design synchronous counter with lower ODC. The existing Hyb DPWM-SPSE-DL attains moderate performance of ODC over existing Hyb DPWM-DLP ign. If how it is, the proposed HRDPWM-RSSC-PSC design outperforms existing designs by attaining lesser ODC. For example, the existing Hyb DPWM-SPSE-DL attains maximal ODC 0.78, existing Hyb DPWM-DLP attains 0.76 minimal ODC. But, the proposed HRDPWM-RSSC-PSC attains better outcome with 0.99 lesser ODC. The proposed HRDPWM-RSSC-PSC design provides 23.43%, 32.09% lower ODC compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

The performance of Time Resolution of the existing designs, such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP are ineffectual to design synchronous counter with lower Time Resolution. The existing Hyb DPWM-SPSE-DL attains moderate performance of Time Resolution over existing Hyb DPWM-DLP design. The proposed HRDPWM-RSSC-PSC outperforms existing designs by attaining lesser Time Resolution. For example, the existing Hyb DPWM-SPSE-DL attains maximal Time Resolution 600, existing Hyb DPWM-DLP attains 90 lesser Time Resolution. But, the proposed HRDPWM-RSSC-PSC attains better result with 40.1 lesser Time Resolution value. The proposed HRDPWM-RSSC-PSC design provides 32.87%, 26.87% lower Time Resolution compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

The performance of power of the existing Hyb DPWM-SPSE-DL, Hyb DPWM-DLP designs are ineffectual for designing synchronous counter with minimal power. The existing Hyb DPWM-SPSE-DL attains moderate power performance than existing Hyb DPWM-DLP. But, the proposed HRDPWM-RSSC-PSC design outperforms existing designs by attaining lesser power. If how it is, the existing Hyb DPWM-SPSE-DL attains maximal power 20.93, existing Hyb DPWM-DLP attains 29.45. But, the proposed HRDPWM-RSSC-PSC attains 0.213 lesser power value. The proposed HRDPWM-RSSC-PSC design provides 24.85%, 27.93% lower power compared with existing designs, like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively. From the above table, the proposed method reduces the critical path delay with higher linearity.

5 Conclusion

Due to a certain benefits of DC-DC converter digital control, like programmability, enhanced control algorithms is highly inspired nowadays. The coding is activated in Verilog, then the proposed synchronous counter design is synthesised by Xilinx ISE. The performance metrics are examined to examine the performance of the proposed method. The proposed design attains lower path delay 24.94%, 28.94%, estimated with existing Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

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