Editorial

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Biographical notes: Angsuman Sarkar is presently serving as an Associate Professor of Electronics and Communication Engineering from the Kalyani Government Engineering College, West Bengal. He served as a Lecturer from the Jalpaiguri Government Engineering College, West Bengal of ECE Department for nine years. He received the MTech in VLSI and Microelectronics from the Jadavpur University. He completed his PhD from the Jadavpur University in 2013. His current research interest span around the study of short channel effects of sub 100 nm MOSFETs and nano device modelling. He is a life member of the Indian Society for Technical Education (ISTE) and Institution of Engineers in India. He is also a senior member of IEEE and currently the Chair of Electron Device Society, Kolkata Section. He has authored many books and a number of research papers in national and international refereed journals and conferences.

Swapnadip De graduated in Radio Physics and Electronics from the University College of Science and Technology in 2001. He obtained his MTech in VLSI and Microelectronics from the Jadavpur University. Later, he was awarded a PhD in Engineering from the Jadavpur University. He is a senior member of IEEE and is currently the Secretary of IEEE EDS Kolkata Chapter. He is an executive member of IEEE EDS Kolkata Chapter since December 2013. He is presently working as an Assistant Professor from the Department of ECE, Meghnad Saha Institute of Technology since December 2002.

Over the years, due to the continuous scaling of device dimensions and by the introduction of the new technological nodes, short-channel-effects, variability, leakage power and other various non-ideal effects has become a major concern for further scaling and integration of CMOS technology. The simulation, modelling and characterisation of these non-ideal effects have become extremely important in order to sustain the historical cadence of CMOS scaling. The purpose of this special issue is to present some significant results from recent research studies in the field of 'Devices for integrated circuits'.

This special issue consists of 11 articles carefully selected from the papers presented at the 'Devices for integrated circuits (DevIC 2017)' conference held on 23–24 March 2017 at Kalyani Government Engineering College, Kalyani, India. The guest editor has selected the most interesting works and asked the authors to submit an extended version for publication in this special issue of the *International Journal of Nanoparticles* on: 'Nanotechnology-based devices and nanostructures'. They would like to thank the authors and reviewers for their work in submitting and reviewing the manuscripts. They would also like to thank the Editorial Office of *International Journal of Nanoparticles* for their sincere and patient work. We hope that you will find this special issue interesting and that you will consider participation in the future 'DevIC' conferences.