Introduction

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Biographical notes: Belgacem Ben Hedia holds an Engineering degree in Computer Science from the Faculty of Science, Mathematics, Physics and Natural at the Tunis-El Manar University. He received his PhD in Computer Science from the INSA-Lyon. After his first job in a startup in 2010, he joined the CEA LIST as a research engineer expert since 2015. His expertise covers modelling and validation of real-time and embedded systems. He currently works on the design of safety real-time applications, correct-by-construction code generation and verification of real-time applications and the design space exploration tools (QuaRTOS-DSE) of SW architecture for safety real-time application. He has served in the program committee of several international conferences and workshops dedicated to real-time applications. He was the co-General Chair of RTNS 2014 and Program co-Chair of VECoS 2015. He is the steering committee member of the International Conference on Verification and Evaluation of Computer and Communication Systems (VECoS).

Kamel Barkaoui received his PhD in Computer Science from the Université Pierre et Marie Curie (UPMC) in 1988. He is currently a Full Professor at the Conservatoire National des Arts et Métiers (CNAM). His research interests include formal methods for verification, control and performance evaluation of concurrent and distributed systems. He served on PCs and as the PC Chair for numerous international workshops and conferences. He was the General Co-Chair of the 18th International Symposium on Formal Methods (2012) and General Chair of 35th International Conference on Application and Theory of Petri Nets and Concurrency (Petri nets 2014) and the 14th International Conference on Application of Concurrency to System Design (ACSD 2014). He was the guest editor of *Journal of Systems and Software* (*JSS*) and of *Formal Aspects of Computing* (*FACJ*). He is the Steering Committee Chair of the Int. Conference on Verification and Evaluation of Computer and Communication Systems (VECoS).

This issue is devoted to extended versions of selected contributions dealing with 'Model checking & fault tolerance' accepted and presented in editions of International Conference on Verification and Evaluation of Computer and Communication Systems (VECoS) held in 2015 in Bucharest and 2016 in Tunis.

VECoS was created by a Euro-Med network of researchers in computer science. The aim of the VECoS conference is to bring together researchers and practitioners, in the areas of verification, control, performance, quality of service, dependability evaluation, in order to discuss the state-of-the-art and the challenges in modern computer and communication systems in which functional and extra-functional properties are strongly interrelated. Thus, the main motivation for VECoS is to encourage the cross-fertilisation between the various formal verification and evaluation approaches, methods and techniques, and especially those developed for concurrent and distributed hardware/software systems. Beyond its technical and scientific goals, another main purpose of VECoS is to promote collaboration between participants in research and education in the area of computer science and engineering. We welcome contributions describing original research, practical experience reports and tool descriptions/demonstrations in the areas of verification, control, performance, quality of service and dependability evaluation.

The program committees included researchers from 15 countries and more than 40 laboratories. Each of the 45 submitted papers was evaluated by at least three reviewers. Afterwards, reports returned to the program committee for discussion and resolution of conflicts. Based on their recommendations, we selected 21 papers. The proceedings including these accepted papers were published by the CEUR-WS.org. After that, we invited 17 authors to submit extended versions of their papers. After additional refereeing and further revisions, we were able to accept ten papers for inclusion in this special issue. Part 1 'Model checking & fault tolerance' comprises the following papers:

- 'Model-based specification and validation of the dual-mode adaptive MAC protocol'

  Admar Ajith Kumar Somappa, Lars M. Kristensen and Andreas Prinz propose an approach to develop a rigorous specification of the DMAMAC protocol using timed automata and the supporting Uppaal software tool. The Uppaal tool is also used to verify key functional and real-time properties of the protocol. Finally, execution sequences from the formal specification model are used to validate an OMNET simulation model used for performance evaluation of DMAMAC, and to validate a NesC implementation of the protocol on the TinyOS platform.

- 'Fault diagnosis of discrete-event systems based on the symbolic observation graph'

  Abderraouf Boussif, Mohamed Ghazel and Kais Klai propose an efficient approach to construct a symbolic diagnoser. The proposed approach consists in constructing a diagnoser based on the symbolic observation graph (SOG), which combines symbolic and enumerative representations in order to build a deterministic observer from a partially observed model. The SOG was firstly used for the formal verification using event-based model checking as an efficient alternative to the Kripke structure. Besides, the construction of the diagnoser as well as the verification of diagnosability is performed simultaneously on the fly, which can considerably reduce the generated state space of the diagnoser and thus the overall running time.

- ‘A formal model for the analysis and verification of a pre-emptive round-robin arbiter’

  Imene Ben Hafaiedh, Maroua Ben Slimane and Riadh Robbana propose a formal model for the analysis and validation of the round-robin protocol, which is considered as the most widely adopted scheduling algorithm, in particular for real-time applications. The contribution is first to propose a high-level formal, distributed and scalable model for round-robin arbiter based on the notion of timed automata. We then employ model checking, to verify a set of relevant properties of the round-robin protocol such as deadlock freedom and invariant

- ‘Formal verification of intermittent fault diagnosability of discrete-event systems using model-checking’

  Abderraouf Boussif and Mohamed Ghazel propose a formal verification of intermittent fault diagnosability in discrete-event systems. The system is modelled by a finite state automaton and intermittent faults are defined as faults that can automatically recover once they have occurred. Two definitions of diagnosability, regarding the detection of fault occurrence within a finite delay and the detection of fault occurrence before its recovery, are discussed. The diagnosability is analysed on the basis of the twin-plant structure, which is encoded as a Kripke structure, while diagnosability conditions are formulated using linear temporal logic (LTL).

- ‘Using temporal logics for specifying weak memory consistency models’

  Maximilian Senftleben and Klaus Schneider propose the use of temporal logic to describe the behaviour of memory systems. In particular, the use of LTL defines the weak memory models. Thereby, authors easily check the properties of a multithreaded program against several different consistency models and determine the weakest consistency guarantees required to fulfil the given specification.

We are grateful to all the members of the program, organising committees and referees of the proceedings of this special issue for their hard work. The support and encouragement of the steering committee were invaluable assets. Finally, we would like to thank all the authors of the invited and submitted papers and all the participants of these editions.