# Editorial

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**Biographical notes:** P. Karthigaikumar completed his PhD in Information and Communication Engineering under Anna University, India in 2011. He is a member of IEEE (MIEEE), and a senior member of Association of Computer Electronics and Electrical Engineers (ACEEE). He received IETE K.S. Krishnan award for the best system-oriented research paper in the year 2010. He applied for two Indian patents and is published in Indian Patent Journal. He is a reviewer for different reputed journals like Elsevier, Wiley, Inderscience, etc., and he has been the Guest Editor for few special issues in Hindawi, Elsevier, Inderscience, and Springer. His research interest includes FPGA implementation of media security algorithm and signal processing algorithm.

Anand Paul is currently working in The School of Computer Science and Engineering, Kyungpook National University, South Korea. He received his PhD in the Electrical Engineering at the National Cheng Kung University, Taiwan, R.O.C. in 2010. His research interests include algorithm and architecture reconfigurable embedded computing. In 2004 to 2010, he has been awarded Outstanding International Student Scholarship, and in 2009, he won the best paper award in national computer symposium, Taipei, Taiwan. He serves as a reviewer for *IEEE Transactions on Circuits and Systems for Video Technology*, *IEEE Transaction on System, Man and Cybernatics*, *IEEE Sensors*, *ACM Transactions on Embedded Computing Systems*, *IET Image Processing*, *IET Signal Processing* and *IET Circuits and Systems*. He is also an MPEG Delegate representing South Korea.

N.M. Siva Mangai completed her PhD in Information and Communication Engineering under Anna University, Chennai, India in 2011, focusing on Power optimisation and failure detection techniques for memory. She is a member of VLSI Society of India (VSI), International Association of Engineers (IAENG), International Association of Computer Science and Information Technology (IACSIT), and The Society of Digital Information and Wireless Communications (SDIWC). She is currently working as an Associate Professor in Electronics and Communication Engineering, Karunya University, Coimbatore, India.

Welcome to this special issue of *IJHPSA*. This issue contains a collection of the best papers out of various authors who have been submitted to this issue. The main goal for this issue is to publish selected research papers from practitioners and academia in innovative architectural aspects and novel techniques for development of related theory, algorithm and case studies arising in the area of next generation smart embedded systems.

The authors of the first paper presented a technology dependent optimised bit parallel multiplier and proved that their algorithm gives improvement in resources, delay and power.

In the second paper, the authors designed a slider to avoid the deadlock in online. It is also evaluated and validated with benchmarks.

In last paper, the authors proposed a technique to generate the test patterns for multiple faults to reduce the power consumption during test time. The authors used ZBDD method to generate the test patterns.