Editorial

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We are delighted to welcome you to the second issue of *International Journal of Circuits and Architecture Design* (*IJCAD*). *IJCAD* is a peer-reviewed international journal with a key objective of providing the academic and industrial communities with a medium that presents original cutting edge research related to the role of circuits, architecture design in electronic design automation.

Rapid developments and convergence in consumer electronics have made the theory of VLSI circuits a burgeoning area of research and development. The *International Journal of Circuits and Architecture Design* (*IJCAD*) proposes and fosters discussion on circuits, architecture design, systems, processor architecture and electronic design automation.

The journal provides a platform for research scholars, scientists and academicians worldwide to promote share and discuss the various new issues and developments in different areas of circuits, architecture and design.

The objectives of the journal are to disseminate new knowledge and technology among the academic and research communities, professionals and industry practitioners, thus bridging the gap between research theories and actual implementation. The journal represents a current, comprehensive and practical information tool in the area of circuit and architecture design.

IJCAD intends to publish original and unpublished work that describes current research in circuits and architecture design on both the theoretical, methodological and fabrication aspects, as well as applications. *IJCAD* is published quarterly (four issues every year). *IJCAD* publishes two types of articles: regular papers and brief (short) papers.

Regular papers describe recent fundamental contributions in the field of circuits and architecture design. Brief papers are targeted for the rapid publication of special short communications. Each manuscript is thoroughly reviewed by three or more independent reviewers. The journal policy is to notify the authors with the review result within 90 days of receipt of their papers.

We received several paper submissions, which were all peer-reviewed by 20 professional reviewers. Finally, five submissions were accepted for publication in second issue.

The first paper titled ‘PGC: a pattern-based graphics controller’ presents a SoC design for pattern-based graphics controller (PGC) that handles graphics peripherals efficiently. The proposed system is highly reliable in terms of cost, performance and power. The PGC-based system is implemented and tested on a Xilinx ML505 FPGA board. The PGC

is able to captures video at 2.5×, 1.78× and 5× of higher frame rate and achieves 1.8× to 14.6× of speedup while executing different image processing applications. Authors have also reported that PGC is power efficient.

The second paper titled 'A heuristic approach to variable ordering for logic synthesis engine design: algorithmic insight' presents discussion on logic synthesis. In this paper, authors have presented investigation and analysis on vide detailed insight into a state of the art minimisation algorithm employing data structure to form the basis for synthesis engine. Also, a step by step of a binary decision diagram (BDD) formation and reduction and will analyse in detail for optimal and enhanced performance is presented.

Third article titled 'Design of fractional order integrators and differentiators using novel rational approximations' presents a new improved rational approximations based on Halleys iterative method incorporating different orders of one-half, one-third and one-fourth fractional order integrators (FOIs) and fractional order differentiators (FODs). The proposed technique has been observed to gear up towards more efficient discretised models when compared with those of existing well established approximation techniques.

Fourth article titled 'Assertion based functional verification analysis of AMBA-AHB using System Verilog' demonstrates a widely used advanced microprocessor bus architecture (AMBA) and the verification model using System Verilog.

Fifth article titled 'An efficient arbitration technique for system-on-chip communications' presents a very interesting area of arbitration. In this paper, authors have presented an efficient arbitration technique for SoC communications. The design has capability to programme the priority of any request dynamically. The architecture of the presented design is based on programmable priority encoder to rotate the priority. The maximum operating frequency obtained is 415 MHz.

We would like to take this opportunity to thank all the people who have helped in releasing the second issue. We are also grateful to all our editorial board members who provided us with a lot of support and advice, and who will continue to support us in the coming years. All of them are established researchers in their field and we are sure that their international reputation and great expertise in the field of circuit, architecture and design will have a significant contribution in shaping up *IJCAD* as a reputed international journal.

We are honoured and fortunate to work with a strong technical editorial team of Inderscience Enterprise Ltd.

Our special thanks go to all the authors who have contributed papers to the inaugural issues of *IJCAD*. We hope to build *IJCAD* so that it becomes a central forum for the circuits and architecture design community and one of the main media for presenting original research ideas. We encourage researchers from all disciplines and specialties to submit their papers, as well as reviews, and letters to the editor.

Thanks again for all your encouragement and support. We look forward to working with you.