Introduction

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Biographical notes: Nader Bagherzadeh has been involved in research and development in the areas of computer architecture, reconfigurable computing, VLSI chip design and computer graphics. He was the Chair of the Department of Electrical and Computer Engineering in the Henry Samueli School of Engineering at the University of California, Irvine. Before joining UC, Irvine, from 1979 to 1984, he was a member of the Technical Staff (MTS) at AT&T Bell Laboratories. As a Professor, he has published more than 200 articles in peer-reviewed journals and conference papers in areas such as advanced computer architecture, system software techniques and high performance algorithms.

For this special section of the *International Journal of High Performance Systems Architecture*, we have selected four papers that address two important topics for high performance computing: network-on-chip (NoC) and reconfigurable computing. The growing demand for multi-core computing and software-based solutions for computation intensive applications that previously were only possible by using hardwired architectures, such as ASICs, have steered research and development towards these two areas of computer architecture. These four papers originally appeared in the ITNG 2009 Conference, which was held in Las Vegas, Nevada. All in all authors of six papers from this conference were invited to submit extended versions of their paper for this special section. All these papers went through an extensive peer review where at least three reviews were obtained for each paper. The four papers that appear in this section were selected for publication in the journal.

The paper titled 'A networks-on-chip emulation/verification framework', provides a hardware/software NoC open platform emulation framework for speeding up simulation time while maintaining cycle accuracy of the NoC architecture modelling effort. As the complexity of NoC based architectures increases, having an efficient emulation and verification framework becomes a necessity. In the paper titled 'A scheduling approach for distributed resource architectures with scarce communication resources', authors propose an approach based on list scheduling for single threaded tasks onto a distributed architecture. Their approach statically at compile time determines placements, communication routes, and schedule of operations. Authors of the paper titled 'A unified design space simulation environment for network-on-chip: fuse-N', describe a unified simulation framework for NoCs which simplifies the design space exploration for these type of architectures by providing a comprehensive simulation support. Finally, in the paper with the title 'Reconfigurable processor based on ALU array architecture for software radio', researchers design and prototype software radio system for consumer electronics applications.