Editorial

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Biographical notes: Mohamed Khalgui is a Researcher at Xidian University in China. He was a Full-Time Researcher in Computer Science at Martin Luther University in Germany, a Part-Time Researcher at ITIA-CNR Institute in Italy, a Collaborator with SEG Research Group in Greece, and a Lecturer at Henri Poincaré University as well as EEIGM Institute in France. He obtained the Bachelor Degree in Computer Science at Tunis University in 2001. The master degree was obtained in telecommunication and services at Henri Poincaré University in 2003. He made research activities in Computer Science at INRIA Institute to obtain the PhD at the French Polytechnic Institute of Lorraine in 2007. He participates in several European Projects and also in other interesting international collaborations. He is currently Head of ICTICA.

Hans-Michael Hanisch is Head of the Research Laboratory on Automation Technology at Martin Luther University in Germany. He obtained in 1982 the diploma degree on Chemical Engineering with Excellent, and in 1987 the PhD diploma with 'summa cum laude' on 'Mathematical Modelling of Discrete Control Tasks in Chemical Process Systems' at Polytechnic Institute of Leuna Merseburg in Germany. Between 1991 and 1993, he followed researches in the Process Control Laboratory at University of Dortmund in Germany to prepare the Habilitation which was successfully obtained in 1995. He is an active member in several scientific international organisations and supervises different R&D projects as well as PhD works. He wrote more than 180 papers in reviewed Journals and Conference Proceedings.

Embedded systems are generally defined as computer systems that apply dedicated functions often with real-time computing constraints. They are embedded as parts of complete devices often including hardware and mechanical parts. By contrast to general computers such as personal computers, they are designed to be flexible and to meet a wide range of end-user needs.

Nowadays, the development of embedded software is not a trivial and easy activity because they have classically to satisfy user requirements in addition to their time to market that should be shorter than ever. We are interested in this Special Issue in Modelling, Verification, Scheduling, Implementation and Reconfiguration of Embedded Software.

The first paper 'Formal approach for the development of intelligent industrial Control Components' deals with reconfigurable embedded control systems following different component-based technologies and/or Architecture Description Languages used today in industry. The authors define Control Components as software units to support control tasks of the system which is assumed to be a network of components with precedence constraints. An agent-based architecture is proposed to handle automatic reconfigurations under well-defined conditions by creating, deleting or updating components to bring the whole system into safe and optimal behaviours. To cover all reconfiguration forms, the agent is modelled by nested state machines according to the formalism Net Condition/ Event Systems (NCES). A model checking is applied to verify functional and extra-functional properties of NCES according to the temporal logic 'Computation Tree Logic' (CTL), in order to check the agent's reactivity after any environment's evolution. Several complex networks can implement the system where each one is executed at a given time when a corresponding reconfiguration scenario is automatically applied by the agent. To check the correctness of each one of them, a refinement-based approach is automatically applied in several steps to specify feasible Control Components according to NCES. The model checker SESA is automatically applied in each step to verify deadlock properties of new generated components, and it is manually used to verify CTL-based properties according to user requirements. The reconfiguration agent is implemented by three modules that allow

interpretations of environment's evolutions, decisions of useful reconfiguration scenarios before their applications.

The second paper 'Virtual start-up of plants using formal methods' deals with start-up of a manufacturing system which is a time-consuming task because control software is usually designed from the real plant or a simulation model. Even the most experienced software engineer is not able to consider every possible scenario without having feedback from a plant or its model. So, undesired behaviour can occur after transferring software to the controller. At best, the errors are recognised just after starting-up, so that the software can accordingly be corrected. But there can be even worse failures that occur rarely and randomly, but are the more critical and mean danger for human and machine. This problem is of high significance because automated systems get more and more complex, especially if they control parallel operations. Hence, control software bugs are pre-assigned and should be considered in early project phase. The paper's approach presents an integrated framework that facilitates virtual start-up of a plant. For this, formal methods are applied, so that control software cannot only be simulated but also verified before start-up. This eases control software design and reduces plant downtimes and consequently costs.

The third paper 'Combining formal methods for the development of reactive systems' deals with the use of two verification approaches: theorem proving and model checking. The authors focus on the Event-B method by using its associated theorem proving tool (Click n Prove), and on the language TLA+ by using its model checker TLC. By considering the limitation of the Event-B method to invariance properties, the paper proposes the use of the language TLA+ to verify liveness properties of a software behaviour. The authors extend first of all the expressivity and the semantics of a B model (called temporal B model) to deal with the specification of fairness and eventuality properties. Second, they give transformation rules from a temporal B model to a TLA+ module. The paper presents a prototype system called B2TLA+ that supports this transformation; then verifies these properties of finite state systems with the model checker TLC. For the verification of infinite-state systems, the authors propose the use of the predicate diagrams.

The fourth paper 'Evaluation of meta-heuristic approaches for scheduling optimisation of Flexible Manufacturing Systems' deals with Computer Integrated Manufacturing (CIM) technologies which is a real-time computerised integration of manufacturing activities (Design, Planning, Scheduling and Control) to produce right products at right time. The productivity of CIM is highly depending on the scheduling of Flexible Manufacturing System (FMS). Shortening the makespan leads to decreasing machines idle time. Conventional methods of solving scheduling problems such as heuristic methods based on priority rules still result schedules, sometimes, with significant idle times. To reduce these, the authors propose a meta-heuristic approach called Ant Colony Optimisation (ACO) method for scheduling optimisation of Flexible Manufacturing Systems by considering multiple objectives i.e., minimising the idle time of the machine and minimising the total penalty cost for not meeting the due date concurrently. The results available for the various existing meta-heuristic methods are compared with results obtained by ant colony optimisation method.

The fifth paper 'Incremental verification of component-based timed systems' deals with the incremental development by integration of components of component-based timed systems. This research work is interested in particular in the preservation of their properties during the development process. The authors model timed components with timed automata. Their composition is achieved with the classic parallel composition operator for timed automata. The specification of these timed systems are expressed with the timed linear logic Mitl (Metric Interval Temp oral Logic). To guarantee the preservation of properties during an incremental development process, the authors propose simulation relations adapted for timed systems. First, they extend the classic notion of simulation with timed aspects. As in the untimed case, this relation called timed simulation preserves safety properties. To preserve more constraints, in particular liveness ones, the paper presents another relation, called divergence sensitive and stability-respecting (DS) timed simulation. This last relation preserves all Mitl properties (and thus liveness ones), but also strong non-zenoness and deadlock-freedom. Moreover, the authors study if the relations are appropriate to the use of the composition operator that they consider. For this purpose, the paper studies if the relations are compatible with this operator, and if composability and compositionality hold. These three properties are a way to reduce the cost of the verification of the preservation, or even to get it for free. It results that the timed simulation is appropriate with the classic operator since the properties hold without any assumption. However, this is not the case for the DS timed simulation.

The sixth paper 'Real-time reconfigurable SoC for process control' deals with Hard Real-Time (RT) embedded power control which is an appropriate application area where a skilled balance between hardware and software competencies is particularly important. The aim of this paper is to present a methodology based on novel Field Programmable Gate Array (FPGA) integrating powerful embedded processor cores with embedded RT kernel, applied to the implementation of control algorithms. This methodology is used in electric motors drive in order to enhance both flexibility and performance. Various architectures based on the hard-core PowerPC405 or the soft-core Microblaze combined with reconfigurable logic and dedicated resources on the FPGA have been contrasted in terms of speed and area. The paper describes an approach for balancing control algorithms distribution between hardware and software in the same System on Chip (SoC).

The seventh paper 'A multi-level design methodology of Multistage Interconnection Network for MPSOCs' proposes a design methodology of multistage interconnection

networks for multi-processor system on chip. The framework covers the design step from algorithm level to RTL. The authors first develop a functional formalisation of MIN-based on-chip network at a high level of abstraction. The specification and the validation of the model have been defined in the logic of ACL2 proving system. The main objective in this step is to provide a formal description of the network that integrates architectural parameters which have a huge impact on design costs. After validating the functional model, step 2 consists in the design and the implementation of the Delta multistage networks on chip dedicated to multiprocessor architectures on reconfigurable platforms FPGA. In the last step, the authors propose an evaluation methodology based on performance and cost metrics to evaluate different topology of dynamic network through applications with different number of cores. The paper also shows in the proposed framework that multistage interconnection network will become future general purpose communication architecture for MPSOCs.

Finally the last paper 'Nominal decomposition of colour space transformation for the computer system for the reconfigurable computing and SA-C programming' proposes a nominal decomposition to compute the colour space transformation in single assignment C language to shorten the execution time. The chromaticity coordinate transformation will be used by using fixed-point nominal decomposition. The look-up table for the gamma curve function mapping is also developed by illustrating two Taylor expansion types. The variables are decomposed into two corresponding values: nominal value and base value. K-Table matrices with respect to different bases are also derived to provide the base transformation. The proposed algorithm is appropriate for the single assignment C programming. The VHDL codes can be automatically programmed by using Data Flow Graph in SA-C compiler. The numerical results will verify that the developed algorithm can save the execution time. The developed algorithm can be very useful to implement the computer display and printer system in the firmware interface aspects.

Acknowledgements

We would like to thank Prof. Dr. Quan Zhu who is Editor-in-Chief of *International Journal of Computer Applications in Technology* (IJCAT) for the acceptance of our Issue in the Journal, for useful services and fruitful collaborations.