Preface

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With the progress and popularisation of embedded systems in the past few years, efficiency, instead of functionalities, has become an important factor in measuring the value of embedded systems. How to efficiently use the limited resources in an embedded system to obtain optimal performance has also become a very important issue. Reconfigurable and multi-core architectures are promising solutions to this issue. Compared to conventional hardware with fixed functionalities, reconfigurable hardware has better flexibility in using the limited resources in an embedded system. For the same amount of computing resources, conventional hardware can provide a single set of functionalities only. However, reconfigurable hardware can reuse the same resources to provide multiple sets of functionalities at different time points. Developers of embedded systems can also use the reconfigurable technology to satisfy system requirements such as small area, high performance, and low power consumption. The reconfiguration technology is especially suitable for implementing run-time systems such as wireless sensor applications. In the conventional single-core architecture, all loads of computation burdened the only core and the performance is limited to a critical point. This limitation is solved by the multi-core architecture. In the multi-core architecture, all of the cores can share the loads to achieve load balancing and improve the performance substantially by exploring the parallelism of computations. Since adopting both reconfigurability and multi-core architectures can achieve high performance, how to integrate these two-technologies to achieve much higher performance is an attractive research issue. This special issue is mainly a collection of experiences in reconfigurable computing technologies, multi-core embedded systems, and the integration of the two research areas.

We received several paper submissions, which were all peer-reviewed by 15 professional reviewers. Finally, nine were accepted for publication in this special issue. Among these, seven belong to the reconfigurable research area and two belong to the multi-core-related research area. The topics of the submitted papers in the reconfigurable research area include overview and framework of reconfigurable systems, system level design, RTL code generation, architecture synthesis, and applications. The first paper in the reconfigurable research area gave an overview of reconfigurable systems, which introduces the research issues, the potential limitation in such a system, and the possible solution, adopting self-adaptive and autonomic computing systems. The second accepted paper proposed a framework of reconfigurable systems, which uses the conception of virtual resources to design embedded system. The third paper is related to system level design, which proposed a hardware task placer. Compared to the traditional placer which could only achieve one goal, the novel placer could satisfy multi-objective simultaneously. The fourth paper is related to RTL code generation, which presented a complete design flow to implement dynamically reconfigurable SoCs by moving from high level MARTE models to automatic code generation. The fifth paper belongs to architecture synthesis area, which proposed a novel methodology to achieve a cost-effective reconfigurable system solution. The sixth and seventh papers applied the reconfigurable technology in low power cache design and image security application, respectively. The topics of the submitted papers in the multi-core related research area include programming model and simulator design of multi-core systems. The eighth accepted paper proposed a programming model of multi-core systems, which provides a higher abstract level to control the communication and execution of multi-core hardware, while the attached development tools help developers to debug applications and measure the performance of applications. The last accepted paper proposed a simulator which hybridised two-multi-core architectures for multi-program and multi-core (MPMC) paradigm and single-program and multi-core (SPMC) respectively. The simulators could provide preliminary results to evaluate the performance of the hybrid multi-core processor for both multithreaded and single-threaded programs.

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