Editorial

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Biographical notes: Srikanta Patnaik is Chairman and Founder Director of Interscience Institute of Management and Technology, Bhubaneswar, India. He received his PhD in Engineering in the year 1999 from Jadavpur University, Calcutta, India. He has authored the book *Robot Cognition and Navigation: Experiment with Mobile Robot* and edited two volumes: *Machine Learning and Perception* and *Innovations in Robot Mobility and Control* published from Springer, Germany. His name has been placed in the *Marquis Who's Who in the World for the 2004*. He has been nominated as the International Educator of the Year 2005 by International Biographical Centre, Great Britain.

N.P. Mahalik is presently working as Visiting Professor in the Department of Industrial Technology, California State University, Fresno, USA. He completed his BSc Engg and MEng in the year 1989 and 1993, respectively from UCE, Burla in India. He has been awarded with PhD from De Montfort University UK in the year 1998 for his research contribution in the field of distributed control systems. He has published several research papers, books and papers in the field of mechatronics, process control and automation. He has completed many projects sponsored by various sponsoring agencies. He is the recipient of the Brain Korea 2004 fellowship.

Welcome to Vol. 2, Nos. 1/2 of *International Journal of Information and Communication Technology*. This issue brings articles from *First International Conference on Electronic Design 2008, ICED2008* held in Malaysia during Nov. 2008, on IT applications in embedded applications and design.

The first paper of this issue entitled 'Experiments on data processing algorithms: energy efficiency of wireless and untethered field programmable gate array (FPGA)-based embedded systems' by Pawel Piotr Czapski and Andrzej Sluzek explains the data processing approach to energy efficiency of wireless and untethered FPGA-based embedded systems. They have presented addressing local data processing versus communicating processed data that are envisaged to decrease the total energy spent on communicating data bits.

The second paper 'Design of resolution adaptive TIQ flash ADC using AMS 0.35μm technology' by G. Rajashekar and M.S. Bhat presents a resolution adaptive flash A/D converter design and its performance. Their proposed model is a true variable resolution ADC, operating at 3-bit, 4-bit, 5-bit and 6-bit precision depending on control inputs.

The third paper 'A novel economical duty cycle division multiplexing with electrical multiplexer and demultiplexer for optical communication systems' by G.A. Mahdiraji et al. explains a duty cycle division multiplexing (DCDM) as an alternative multiplexing technique. In their paper, they have examined three channels each operating at 10 Gb/s over a single optical carrier.

The fourth paper entitled 'Lossy compression and curvelet thresholding for image denoising' by G. Jagadeeswar Reddy et al. explains a new system of multiscale transform, namely, the curvelets, which possess directional features and provides optimally sparse representation of objects with edges. In this paper an algorithm for image denoising based on lossy compression and curvelet thresholding (LCCT) is proposed.

The fifth paper entitled 'Run-time management of custom instructions on a partially reconfigurable architecture' by Siew-Kei Lam et al. explains a scheme for managing the run-time reconfiguration of custom instructions on a partially reconfigurable architecture that incorporates multi-bit logic blocks.

The sixth paper entitled 'A tightly coupled finite field arithmetic hardware in an FPGA-based embedded processor core for elliptic curve cryptography' by Mohamed Khalil-Hani et al. explains the implementation of a tightly-coupled hardware architectural enhancement to the Altera FPGA-based Nios II embedded processor. Their experimental results showed that for the point multiplication operation, which is the core operation in an ECC computation, the implementation with custom instructions and tightly-coupled hardware is about 50% faster than the co-processor based hardware.

The seventh paper 'The effects of compiler optimisations on embedded system power consumption' by Shuhaizar Daud et al. explains that the effects of compiler optimisations on embedded systems energy usage and power consumption in real time situations. They have also highlighted the importance of running efficient binary codes in realising a more power efficient, and better performing embedded system.

The eighth paper entitled 'Accelerating the AES encryption function in OpenSSL for embedded systems' by Vishnu P. Nambiar et al. explains the implementation of a cryptographic (crypto) embedded system, deploying an Altera Nios II embedded processor working with an AES encryption hardware accelerator. Their experimental results showed that hardware acceleration can improve significantly the performance of OpenSSL crypto functions, and hence, of the SSL connection as well.

The next paper entitled 'A low power CMOS voltage reference circuit with subthreshold MOSFETs' by S. Ramasamy et al. explains a novel approach for the design of low power CMOS bandgap reference circuit. Their technique has been validated using both NMOS and PMOS diode connected subthreshold MOSFETs for generating voltages with negative temperature coefficient.

The tenth paper 'SystemC-based HW/SW co-simulation platform for system-on-chip (SoC) design space exploration' by Yuan Wen Hau and Mohamed Khalil-Hani explains the SystemC modelling of the hardware and the software parts of the system, and the inter-process communication module of the co-simulation platform.

The next paper by Joo-Yul Park et al. entitled 'A novel SoC platform based multi-IP verification and performance measurement' explains a novel SoC platform based

verification methodology which tests multiple IPs together using a single testbench. They have proposed a methodology namely embedded processor core built in the SoC device which is used mainly for verification purposes, and runs a C-based testbench.

The twelfth paper entitled 'Optimisation of RunBefore decoder and first one detector for MPEG-4 AVC/H.264 CAVLC decoding' by So-Jin Lee et al. explains a novel RunBefore decoder and a new FOD (first one detector) for MPEG-4 AVC/H.264 CAVLC decoding. Their proposed CAVLC decoder has been designed in Verilog HDL, and synthesised by Synopsys' Design Compiler using MagnaChip 0.18μm CMOS cell library.

The next paper entitled 'Identification of LPI radar signals by higher order spectra and neural network techniques' by L. Anjaneyulu et al. explains the results of HOSA techniques (bi-spectrum, bi-coherence and tri-spectrum) and artificial neural networks (ANNs), applied to LPI radar signals.

The last paper 'Low power reconfigurable sub-band filter bank ASIC for MP3 decoder' by B.P. Gangamamba et al. proposes an architecture, which consumes less power at run time as the last 12 bits of the mantissa part of the synthesis filter coefficients are zero most of the time and hence the corresponding multipliers will be switched off. They have synthesised and simulated the architecture using 0.35 μm process technology under Synopsys environment.