Preface

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Biographical notes: Deepu Talla received his PhD in Computer Engineering from the University of Texas at Austin in 2001. Prior to that, he obtained a Master's Degree in Electrical Engineering in 1998 from Villanova University, PA, and a Bachelor's Degree in Electronics and Communication Engineering in 1996 from Andhra University, Visakhapatnam, India. Currently, he is working for Texas Instruments Inc. as a System Architect responsible for the Definition and Architecture of Portable Multimedia SoCs. He is a member of the IEEE, the IEEE Computer Society, the IEEE Signal Processing Society, and the ACM. His main interests are in the areas of computer architecture, performance evaluation and benchmarking, and SoC design.

The performance requirements of Digital Signal Processing (DSP) and embedded applications are rapidly increasing, but the power and cost budgets are decreasing. Optimisation plays a very important role in managing the conflicting demands. This issue presents seven papers on various issues related to optimising performance, power and cost of DSP and embedded systems. Both hardware and software optimisations are covered in the papers. Some of the papers were selected from the first four ODES (Optimisations on DSP and Embedded Systems) workshops (http://www.ece.vill.edu/~deepu/odes/), and some were received in an open solicitation.

One of the papers presents a profile of several embedded Java benchmarks, unveiling the opportunities for various optimisations. One paper tackles data dependent conditions to enable global source code transformations. Another paper addresses program slicing across hardware-software boundary. A methodology for comprehensive design space exploration of a smart camera application is presented in another paper. Tradeoffs in the design of a software managed scratch pad memory for embedded systems are discussed in another paper. Leakage management in caches related to embedded systems is presented in one paper. Finally, one paper deals with if conversion on embedded VLIW processors.

We hope that the readers enjoy this special issue and take this opportunity to thank all the reviewers.