Preface

Ed F. Deprettere

Leiden Institute of Advanced Computer Science,
Leiden University, Leiden, The Netherlands
E-mail: edd@liacs.nl

Shuvra S. Bhattacharyya

Department of Electrical and Computer Engineering, and
Institute for Advanced Computer Studies,
University of Maryland, College Park, MD, USA
E-mail: ssb@umd.edu

Biographical notes: Ed F. Deprettere is fellow of the IEEE. He received the MSc Degree from the University of Ghent, Ghent, Belgium, in 1968, and the PhD Degree from the Delft University of Technology, Delft, The Netherlands, in 1981. From 1980–1999, he was Professor at the department of Electrical Engineering, Circuits and Systems section, Signal Processing Group. From January 1st, 2000, he is Professor at the Leiden Institute of Advances Computer Sciences, Leiden University, Leiden, The Netherlands, where he is head of the Leiden Embedded Research Center. His current research interests are in system level design of embedded systems, in particular for signal, image and video processing applications, including wireless communications and multimedia. He is editor and co-editor of four books and several special issues of international journals. He is on the editorial board of three journals.

Shuvra S. Bhattacharyya is a Professor in the Department of Electrical and Computer Engineering and the Institute for Advanced Computer Studies (UMIACS) at the University of Maryland, College Park. He is also an affiliate Professor in the Department of Computer Science. He is coauthor or coeditor of four books and the author or coauthor of more than 100 refereed technical articles. His research interests include VLSI signal processing, embedded software, and hardware/software co-design. He received the BS Degree from the University of Wisconsin at Madison, and the PhD Degree from the University of California at Berkeley. He has held industrial positions as a Researcher at the Hitachi America Semiconductor Research Laboratory (San Jose, California), and as a Compiler Developer at Kuck & Associates (Champaign, Illinois).

The current issue and next issue of the *International Journal on Embedded Systems* are organised as companion special issues that are based on the theme of Systems and Architectures for Embedded Processing. These two issues contain a selection of top papers from the 2003 International Conference on Application-specific Systems, Architectures, and Processors (ASAP 2003) and the 2003 International Workshop on Systems, Architectures, Modelling, and Simulation (SAMOS 2003). ASAP and SAMOS (now the International Conference on Embedded Computer Systems: Architectures, Modelling, and Simulation) are two annual forums that focus on technology for design and implementation of embedded systems. ASAP 2003 was located in The Hague, The Netherlands under the organisation of Ed Deprettere and Shuvra Bhattacharyya (General Co-Chairs), and Lothar Thiele, Alain Darte, and Joseph Cavallaro (Program Co-Chairs). SAMOS 2003 was located, as all meetings of this forum have been held, in Samos, Greece. SAMOS 2003 was organised by Stamatis Vassiliadis.

Our two companion issues are organised under the subthemes of Design Methods and Tools (this issue), which covers selected papers from both ASAP 2003 and SAMOS 2003, and Applications and Hardware, which covers additional selected papers from ASAP 2003.

Three papers in this special issue focus on efficient performance estimation. In A Performance/Cost Estimation Model for Large Scale Array Signal Processing System Specification, Alliot proposes an approach targeted towards large scale signal processing systems that is based on hierarchical decomposition of the implementation target as a hierarchy of platforms with associated performance characterisations that are calibrated at the lowest levels of abstraction. Object-oriented models are developed to represent the abstractions for incorporation into design tools. In The Artemis Workbench for System-level Performance Evaluation of Embedded Systems, Pimentel presents a design tool for modelling and mapping between multimedia applications and system-on-chip architectures. Emphasis in the paper is placed on demonstrating a novel dataflow-based, intermediate mapping layer for relating application events to architectural events, and performing accurate architectural exploration. The techniques are demonstrated on a motion-JPEG encoder

application. In Evaluating Memory Architectures for Media Applications on Coarse-Grained Reconfigurable Architectures, Lee, Choi, and Dutt focus on dynamically reconfigurable ALU architectures (DRAAs), which is an emerging class of coarse-grain architectures that is especially well-suited to media applications. This paper analyses the interaction of DRAAs with different forms of memory subsystems, and develops methods for rapid, early-stage performance estimation to guide architectural exploration.

Two papers address power consumption considerations for embedded systems. In Power-Efficient VLIW Design using Clustering and Widening, Pericas et al. examine the impact of various combinations of clustering and widening for functional units, as well as various register file sizes, in VLIW processor designs for media applications. The experiments provide insights into the interactions between these three design factors in relation to overall performance, power consumption, and energy-delay product. In Reducing Dynamic Power Consumption in Next Generation DS-CDMA Mobile Communication Receivers, Chandrasekar, Livingston, and Cavallaro explore algorithmic and architectural design methods and trade-offs for direct sequence code division multiple access (DS-CDMA) receivers. The work centers around evaluating and optimising the impact on power consumption and algorithm performance of reduced numerical precision at the algorithmic level, and both precision and activity rate reduction at the architectural level. For demonstration of the ideas, the techniques are targeted for implementation on a Xilinx Virtex-II FPGA platform.

Two papers study process network models of computation for modelling of applications and architectures. In Deriving Efficient Control in Process Networks with Compaan/Laura, Derrien et al. apply process network analysis to the mapping of MATLAB programs onto FPGA implementations. Specifically, this work develops alternative approaches for deriving hardware control structures to route data between processes in a Kahn Process network, and examines trade-offs among these alternatives in terms of performance and resource requirements. In Context-Aware Process Networks, van Dijk and Sips extend the Kahn process network (KPN) model of computation with a non-determinate construct as a means for representing interfaces to asynchronous events. A useful transformation is then developed from this extended model to a parameterised form of KPN such that traditional analysis methods for conventional (determinate) KPNs can be carried out after the transformation.

Three papers present toolsets and design methodologies for the design of embedded systems. In Virtual Architecture Mapping: A SystemC based Methodology for Architectural Exploration of System-on-Chips, Kogel et al. propose a system level SoC design methodology based on the SystemC 2.0 library. Using the methodology, designers are able to explore high-level, architectural design alternatives with high productivity and simulation speed. In SoC Multiprocessor Debugging and Synchronisation using Generic Dynamic-Connect Debugger Frontends, Wieferink et al. present a toolset that provides capabilities for debugging and profiling multiprocessor system-on-chip systems. The toolset, which is available through CoWare, provides for analysis of models at various levels of abstraction, including SystemC-based specifications of hardware modules, and allows designers to experiment with different trade-offs involving simulation detail, accuracy, and performance. In A HW/SW Design Methodology for Embedded SIMD Vector Signal Processors, Robelly, Cichon, Siedel, and Fettweis, present a design methodology and associated tools for hardware/software co-design involving programmable digital signal processor cores that employ SIMD parallelism. The work allows algorithms to be developed independently of the amount of SIMD parallelism in the target processor, and then to be mapped onto different SIMD configurations through an algebraic framework. Based on this framework, a design flow is presented for mapping MATLAB programs onto the targeted class of vector signal processor cores.

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