# Editorial

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**Biographical notes:** Christian W. Probst is an Assistant Professor in the Department for Informatics and Mathematical Modelling at the Technical University of Denmark. His research interests include language-based security, virtual execution environments, static analyses and optimising compilers and distributed systems. He received Dr. Ing. and Diploma Degrees in Computer Science from Saarland University, Germany.

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In April 2005, a Dagstuhl seminar on 'Power-aware computing systems' was held at the International Conference and Research Centre for Computer Science, Schloß Dagstuhl. The workshop brought together 35 researchers from academia and industry. This special issue presents papers that were selected by a peer-reviewing process from submissions by participants.

In the first paper, 'Power-aware computing systems', we give an overview of the seminar's discussions and results. It is followed by the first group of papers, targeting software-related topics. The first paper, 'Inter-program optimisations for disk energy reduction', investigates the benefits of optimising sets of programs as opposed to individual programs. The experiments show that

inter-program optimisations result in significant energy savings over individually optimised programs. In 'A new way of estimating compute-boundedness and its application to dynamic voltage scaling' the authors propose a new metric for evaluating the performance loss caused by dynamic voltage scaling. The metric is logically related to clock frequency and execution time, namely the percentage drop in cycles caused by reduced frequency. In 'An evaluation infrastructure for power and energy optimisations', the last paper in this group, the authors aim to bring together the advantages of simulation and physical measurement in an evaluation infrastructure for power and energy optimisations. Power and energy behaviour is obtained through physical measurement, but simulation is used for observing the connection between power and energy behaviour and the evaluated program.

The second group of papers targets issues related to design and synthesis of (components of) power-aware systems. In 'Exploring temperature-aware design in low-power MPSoCs' the authors investigate the need for temperature-aware design in a low-power systems-on-a-chip, and provide guidelines to delimit the conditions for which temperature-aware design is needed. It is followed by 'Design of power-aware FPGA fabrics', presenting two techniques to reduce the power consumption in FPGAs. The first technique uses two supply voltages to reduce power while maintaining the design's performance, the second technique targets applications where configuration time is crucial. Main memory has become one of the largest contributors to overall energy consumption and offers many opportunities for power/energy reduction. The authors of 'Power Management in external memory using PA-CDRAM',

propose a new memory organisation, Power-Aware Cached-DRAM, that integrates a moderately sized cache directly into a memory device. This cache allows to turn a memory bank off immediately after a memory access to reduce energy consumption. In the fourth paper, 'Energy-aware compilation and hardware design for VLIW embedded systems', the authors develop a new approach to reduce the power consumption of the register file in VLIW architectures. The register file is one of the key sources of power consumption and its design and management is therefore crucial in designing those systems. The final two papers in this section also target the design and synthesis of lowpower systems. In 'Algorithms for low power hardware synthesis from CAOS: concurrent action oriented specifications' the authors present CAOS as a model with low granularity concurrent atomic action descriptions with a semantics similar to Dijkstra's guarded command language. The low granularity based modelling relieves the designer of the obligation of a priori scheduling of actions, thereby raising the abstraction level of hardware specification. Finally, 'Horizontal and vertical HW/SW co-design flows for power aware smart card designs' presents a HW/SW co-design methodology for the design of resource limited embedded devices in the domain of smart cards. The focus is on the detailed description of the two design flows under the aspect of power awareness.