Editorial

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Biographical notes: Dr. Z.J. Pei is an Associate Professor in the Department of Industrial and Manufacturing Systems Engineering, Kansas State University, teaching courses on manufacturing processes and systems; manufacturing processes for semiconductor materials and devices; statistical quality control; lean manufacturing; and Six Sigma. After receiving his PhD in Mechanical Engineering from University of Illinois at Urbana-Champaign, he worked in industry for four years. He holds three US patents and has published over 30 journal papers and over 60 papers in conference proceedings. His current research activities include analysis and modeling of silicon wafering processes and traditional and nontraditional machining processes.

Dr. Fisher is Chief Scientist for MEMC Electronic Material Inc. He joined MEMC in 1985 and has held various positions including Vice President Corporate Technology, Director of Operations Technology, Technical Operations Manager and Application Engineering Manager. Dr. Fisher has authored or co-authored over 40 papers and two patents. He received a BSc in Physics from the University of Salford in England in 1973 and a PhD in Materials Science from the University of London in 1986. Dr. Fisher is also an Adjunct Professor in the Department of Industrial and Manufacturing Systems Engineering at Kansas State University.

Historically, market growth in the semiconductor industry has been enabled by the increased functionality of successive silicon chip generations. As each generation develops, the number of transistors on a chip doubles, and the number of ways in which these transistors can be configured drives the products that can be developed. This is Moore's Law. Each new generation also requires the ability to shrink the transistor size and this places more demands on the starting wafer features. Wafer surface topography limits the performance of photolithographic methods used to manufacture the semiconductor devices. As feature size decreases, so does the depth of field of the lithography tools and this sets the maximum deviation of the silicon wafer surface from the idealised plane.

As companies compete in a global market with strong downward price pressures, the industry has increased focus on cost reductions. Thus the overall challenge for silicon wafer manufacturers is to produce wafers to very stringent specifications at the lowest possible cost.

Ideally, the process of converting single crystal silicon ingot into flat, smooth and clean silicon wafers should be as simple as possible. Unfortunately the initial process of cutting or slicing an ingot creates defects in the resulting slices such that further downstream processing is required to remove them. The spatial frequency of surface topography features is machine tool dependent. Typically, a number of tools are required to process a slice from the 'as cut' condition to a smooth, flat, clean, mirror polished surface. The goal of ductile machining (without producing surface undulations or subsurface, crystallographic damage) has not yet been completely achieved. Chemical etching leaves a wafer completely free of machining damage, but such wafers do not meet the required surface planarity. Most mechanical machining processes result in some degree of brittle fracture which leads to subsurface damage. The dilemma is that fast, low cost processes tend to create more damage, while gentle processes, operating close to ductile mode and generating little or no damage, tend to be slow and therefore expensive.

The papers presented in this special issue of *IJMTM* deal with both the theory and practice of processes that are either related to or can be applied directly to the semiconductor industry. Understanding the details behind these processes is important from several viewpoints, but it is essential in order for the silicon wafer industry to meet future product quality requirements and to optimise process flows and operating conditions for lower cost. This edition of *IJMTM* is a welcome and timely publication. We would especially like to thank the authors for their dedicated work in writing these papers in responses to our solicitations and the reviewers for their careful and timely help in making a critical assessment of these journal papers prior to publication.