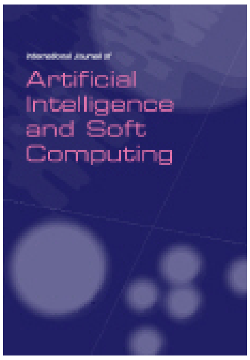

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Integrated AWA fitness PSO-SPICE framework for automated design and optimisation of analogue and mixed-signal ICs

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Abstract: The design and optimisation of analogue and mixed-signal integrated circuits become intractable with technology scaling. It gives rise to multi-dimensional tradeoffs among its numerous performance metrics. Evolutionary algorithms are being explored to generate possible solutions having goodness of fit with the desired solution. In this direction, a novel fitness evaluation function integrated with PSO and PSO-SPICE framework is proposed to design and implement multi-objective optimisation for analogue and mixed-signal circuit design automation. The framework is demonstrated to automatically design and optimise the multi-objectives of 2-stage op-amp and 4-bit flash ADC. The proposed fitness evaluation function demonstrate large design outperformance independent of quality of initial population and requiring no adaptive weights. The novel fitness function driven PSO-SPICE framework exemplifies a robust, scalable, and precise method for multi-objective optimisation of analogue and mixed-signal circuits of varying scale and design complexity.

Keywords: particle swarm optimisation; PSO; 2-stage op-amp; flash ADC; multi-objective optimisation; AWA fitness function.

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1 Introduction

With advancements in transistor scaling, the analogue and mixed-signal circuits are integrated on-chip resulting in a rise in resistive and capacitive parasitics. In contrast with digital circuits, analogue circuits are more vulnerable to parasitic effects, crosstalk, noise, and other non-idealities. With a limited number of digital design tradeoffs, the electronic design automation (EDA) tools have achieved a high degree of maturity. However, with the emergence of system on chip (SoC) implementation, integrating digital, analogue, and mixed-signal circuits, it has become a herculean task for design engineers to design manually and to achieve multi-dimensional tradeoffs between performance metrics of analogue and mixed-signal circuits in the absence of design automation tools. Manual optimisation, in the presence of nonlinear functionalities, results in sub-optimal solutions involving long and tedious process.

In model-based optimisation, with posynomial or polynomial models, the global optimum can be guaranteed with a reduction in the computational cost as compared to that of simulation-based models. The models developed can be reused for further optimisation, but the predicted circuit performances diverge from the actual circuit performances. However, in simulation-based models, the objective functions, constraints, and performance metrics are directly evaluated and optimised by the circuit simulations (Lyu et al., 2018). The variables of circuit design, such as transistor aspect ratios, bias currents, and passive devices, are tuned to meet few metrics at most while trading the remaining metrics to meet the design specifications closely.

The optimisation-based approach explores the design space to find one optimal solution for multiple tradeoffs between performance metrics (Gonzalez-Echevarraa et al., 2017). Metaheuristic algorithms such as genetic algorithm (GA), artificial bee colony (ABC), and particle swarm optimisation (PSO) algorithms are demonstrated in the design of analogue filters and PSO produces few design errors in comparison. For optimisation of analogue ICs, hybrid methodologies involving PSO and radial basis function (RBF) (Garbaya et al., 2018), PSO and gravitational search algorithm (GSA) (Mallick et al., 2017), PSO and GA (Deb and Padhye, 2014) have been reported. Craziness-based PSO (CRPSO) algorithm is used for the design of PMOS driver-based 2-stage comparator and NMOS driver-based folded-cascode op-amp (Sumalya et al., 2019; De et al., 2017). Multi-parameter optimisation based on artificial neural networks (ANN) are demonstrated in the design of 2-stage op-amp (Harsha and Harish, 2020; Lourenco et al., 2018). The combination of ANN with stochastic gradient descent (SGD) and PSO is shown for designing of high-speed ADC (Bansal et al., 2021). g_m/I_d method is applied to speed-up the non-dominated sorting genetic algorithm (NSGA-II) to predict the device geometry and its appropriate bias levels of the operational transconductance amplifiers (Tlelo-Cuautle and Sanabria-Borbon, 2016). In contrast to heuristic methods of GA and simulated annealing (SA), PSO exhibits rapid convergence to the promising regions (Fakhfakh et al., 2010), resulting in computational savings.

This paper presents a novel fitness evaluation function and an evolutionary algorithm like PSO to optimise an analogue and mixed-signal circuits by employing a simulation-based approach. We demonstrate the proposed methodology by taking design optimisation of a 2-stage op-amp and 4-bit flash ADC for illustration.

The rest of the paper is organised as follows: Section 2 describes the multi-objective PSO and the limitations of its existing fitness functions for analogue design. The proposed AWA fitness evaluation methodology for multi-objective optimisation is presented in Section 3. Section 4 describes design equations for the design of a 2-stage op-amp and 4-bit flash ADC. The PSO-SPICE framework for the design automation and optimisation using the proposed AWA fitness function and its implementation is presented in Section 5. While the results are discussed in Section 6, conclusions are summarised in Section 7.

2 Multi-objective PSO

The complexity in solving optimisation problems continues to scale up, requiring diverse optimisation methods to find the optimum either by maximising or minimising an objective function, and there is no remarkable quantitative method regarded as the best for any case. An optimisation technique is always application-specific, opting for an optimisation technique that relies on the nature of the application (Gomes de Almeida and Leite, 2019).

Based on bird flocking, fish schooling, and swarming theory, Kennedy and Eberhart (1995) has introduced PSO methodology for nonlinear functions that employ basic mathematical operators, and the methodology is computationally efficient in terms of both memory requirements and speed.

A swarm or collection of potential solutions known as particles is maneuvered in the solution space, and the information between particles is traded in order to evolve into an optimum solution, meeting the objective function/s. According to the objectives of the problem, the fitness function is evaluated to determine the fitness values of each particle in the swarm. In PSO, irrespective of the equations of the objective functions, their values alone are essential to finding the optimum solution. The velocities associated with the particles administer the transition of particles in the solution space. The particles drift in the solution space getting attracted by the current best solution.

Along with fitness function evaluation, two prominent assessments have been carried out within the swarm to identify,

1 the local best fitness valued solution P_{best} captured till now by any particle in the process

2 the global best fitness valued solution G_{best} obtained by considering the overall particles in the swarm.

Subsequently, P_{best} and G_{best} are revised at each iteration.

P_{best} mimics reminiscence by revoking each individual involvement/experience in action, and the associated velocity alteration assists the individual in retreating to its most delighted point in the past. Meanwhile, G_{best} is similar to the quintessential knowledge that each individual pursues to obtain. How particle swarm optimiser marches towards P_{best} and G_{best} is analogous to GA's crossover and mutation operations.

Consider a $n * j$ dimensional solution space with a swarm of n particles; after evaluating the fitness of particles, P_{best} and G_{best}, the velocity and position vectors are updated as in equations (1) and (2), respectively.

$$V_{(i,j)}^{(m+1)} = wV_{(i,j)}^{m} + c_1 r_1^m (P_{(best(i,j)} - X_{(i,j)}^m) + c_2 r_2^m (G_{best(j)} - X_{(i,j)}^m) \tag{1}$$

$$X_{(i,j)}^{(m+1)} = X_{(i,j)}^{m} + V_{(i,j)}^{(m+1)} \tag{2}$$

where $i = \{1, 2, 3, ..., n\}$, $m = \{1, 2, ..., \text{maximum iteration}\}$, j is the number of items constituting a particle, inertia weight w balances the search exploration between the local and global searches, c_1 and c_2 represents the relative acceleration factor in the direction of P_{best} and G_{best}, respectively. r_1 and r_2 are the random numbers spanning between 0 to 1. $V_{(i,j)}^m$ and $V_{(i,j)}^{m+1}$ are the current and updated velocities of i^{th} particle, respectively.

2.1 Fitness evaluation

In this work, a novel generic multi-objective model is proposed for evaluating the fitness of the solutions. The fitness evaluation of a solution determines how optimal it is to the desired solution. So, each solution has to be given a numerical value to determine its optimality with respect to the desired solution.

When there is a pool of possible solutions for a unique problem, the best solution among them is to be chosen by evaluating the fitness of all the solutions. When each possible solution is applied to a respective problem, the resulting outcomes are tallied with its desired/optimum solution. For a single objective optimisation problem, the solution with the highest valued fitness is chosen from the pool of solutions as the best solution for maximising the single objective, and the solution with the lowest valued fitness is selected as the best solution for minimising the single objective. In multi-objective optimisation, there are two kinds of objectives: maximise a few objectives and at the same time minimise some other objectives. Care needs to be taken while evaluating the fitness of a solution which comprises both maximising and minimising the objectives simultaneously, else the overall efficiency of the fitness will be degraded.

The conventional fitness evaluation functions like Euclidean distance, Manhattan distance are based on distance evaluation of the obtained solution from the target solution and hence, fail to distinguish between multiple solutions in multidimensional solution space that are equidistant from the target solution. Such solutions return the same fitness value making it hard to determine the most optimal solution. The SP fitness function Papadopoulos et al. (2000), based on the ratio of actual error to acceptable error contributions of inequality objectives, may return identical fitness values for multiple obtained solutions making it hard to pick the most optimal solution. The Yu and Mao (2009) fitness function based on the adaptive weights, determines the optimal solution based on the quality of the initial solution and the adaptive weights.

Further, the fitness values alter as the size of the population pool varies. While optimising, the evolutionary algorithms, like PSO, are subjected to iterations for finding the best solution. There are chances of the same solution occurring in two or more iterations, and the best fitness solution may go unnoticed due to change in population pool characteristics in subsequent iterations. Further, in a few instances, the fitness values may replicate in different iterations even though the individual objective of each solution differs.

Hence, there is a need for a fitness evaluation function that determines the optimal solution, *based on its optimality rather than distance-based closeness with respect to the desired solution*, from among multiple obtained solutions *independent of the quality of initial solution* and *without the need for applying adaptive weights*. Thus, the limitations of existing fitness evaluation methods are addressed in the proposed fitness evaluation methodology to be referred to as 'adaptive weight agnostic (AWA) fitness evaluation function'.

3 AWA fitness evaluation methodology

Consider a pool of obtained solutions for a multi-objective design problem which is represented in the form of $n * m$ matrix, where 'n' is the number of solutions, each having 'm' number of objectives. The rows of the matrix represent multiple solutions and the columns represent multiple objectives. The main aim of the AWA fitness is to measure the optimality of the obtained solutions to the desired solution. The possible solution with the highest fitness value is regarded as the best solution in the respective pool of solutions. The steps for evaluating AWA fitness are illustrated below:

Step 1 If an objective is to be maximised, divide the obtained objective by desired objective,

$$Fit_{Maximise(i,j)} = \frac{Obtained_{(i,j)}}{Desired_{(i,j)}}; \tag{3}$$

where i = 1, ..., n and j = 1, ..., m.

Step 2 If an objective is to be minimised, divide the desired objective by obtained objective,

$$Fit_{Minimise(i,j)} = \frac{Desired_{(i,j)}}{Obtained_{(i,j)}}; \tag{4}$$

where i = 1, ..., n and j = 1, ..., m.

Equations (3) and (4) address the issue of simultaneous maximisation of one set of objectives and minimisation of the rest of the objectives.

Combining the matrices $Fit_{Maximise}$ and $Fit_{Minimise}$ of equations (3) and (4) into a single matrix,

$$Fit_{all(n,m)} = \left[Fit_{Maximise}\, Fit_{Minimise}\right] \tag{5}$$

Step 3 If all fitness values of Fitness matrix in equation (5) are greater than 1, all objectives are equally emphasised requiring no action. The fitness of 1 indicates that the obtained solution is equal to the desired solution and close to 1 indicates closeness of obtained solution to the desired solution.

Step 4 If few fitness values in a row of Fitness matrix in equation (5) are greater than 1, such values are limited to a maximum of 1, to avoid over emphasis of any objective at the cost of other objectives. In other words, to avoid objectives with higher fitness value overshadow the objectives of lower fitness value.

Step 5 All negative values are made zero. A negative fitness value is undesirable and hence is made zero to avoid under-emphasis of any objective with respect to other objectives.

Step 6 Generate AWA fitness value for all n solutions:

1 If all the individual fitness values of a solution (i.e., a row) are equal to or greater than 1, then take their mean.

$$\text{i.e., } \forall Fit_{all(i,:)} \geq 1; \text{ where } i = 1, .., n \tag{6}$$

The AWA fitness value of i^{th} solution is given by,

$$Fit_{AWA(i)} = mean(Fit_{all(i,:)}) \tag{7}$$

2 If the above condition fails, then take mean of sum of squares (SS). The AWA fitness value of i^{th} solution is given by,

$$Fit_{AWA(i)} = mean(SS(Fit_{all(i,:)})) \tag{8}$$

It may be observed that in the six-step fitness evaluation, as no adaptive weights are applied in any step, it is referred to as the adaptive weights agnostic (AWA) fitness evaluation methodology. The AWA fitness evaluation is different from conventional distance measure-based fitness evaluation methods in the sense that it involves comparison between obtained solution and the desired solution based on their ratio and not on their difference. Further, the distance-based fitness evaluation allows small outperformance on any objective while large outperformance will be discarded with low fitness value assigned to it. The design outperformance on any objective indicates that the design solution is superior to the desired solution on that metric, irrespective of the nature of optimisation, i.e., maximisation of few objectives and minimisation of rest of the objectives. As AWA fitness evaluation is based on design optimality and not on distance measure, such large design outperformance is recognised with a large fitness value assigned to it by equations (7) and (8), facilitating large design outperformance.

Further, the AWA fitness methodology is generic in nature and can be applied to determine the best optimal solution, where its optimality rather than distance-based closeness with respect to the desired solution is the requirement, over all application domains.

In this work, two fitness calculations of Yu and Mao (2009) fitness evaluation based on weights and SP fitness evaluation based on errors (Papadopoulos et al., 2000) are carried out, and the efficacy of AWA fitness evaluation is illustrated for design automation of analogue and mixed-signal circuits.

4 Design of analogue integrated circuits

4.1 2-stage operational amplifier design

The basic methodology of op-amp design has two specific steps: The first step is building a suitable circuit topology that remains fixed unless there is a change in the specification. The next step involves the selection of W/L ratios of all transistors in the circuit to meet the desired specifications.

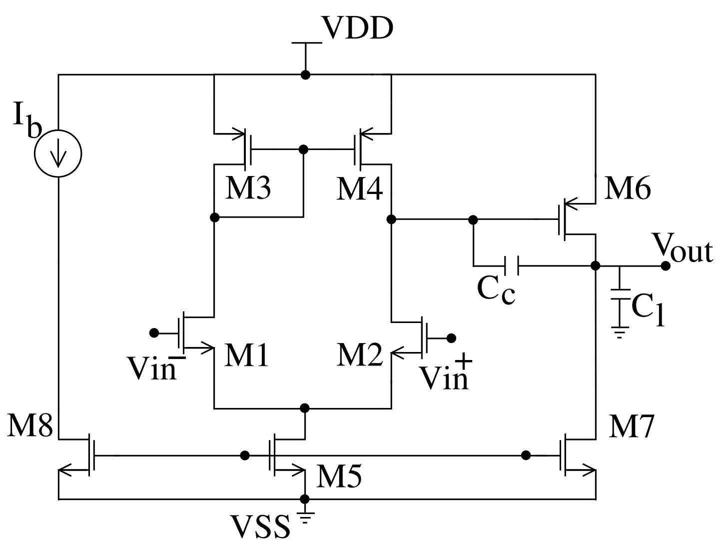
A 2-stage op-amp is designed with the common source configuration as the second stage to contribute large output swings to drive an output device (Ratan et al., 2016). The 2-stage op-amp circuit schematic is as in Figure 1. The performance metrics considered for design are open-loop DC gain (A_v), unity-gain bandwidth ($UGBW$), phase margin (PM), slew rate (SR), power dissipation (P), and area (A). Among these metrics, while gain, bandwidth and phase margin are computed from SPICE output file, the slew rate, power dissipation and area are computed by user defined equations in the SPICE netlist as given by equations (9), (10) and (11) (Allen and Holberg, 2002).

The amount of current that can be bought into the compensation capacitor determines the slew rate, which is given by:

$$SR = \frac{I_5}{C_c} \tag{9}$$

where I_5 is the drain current through M5 and C_c is the frequency compensation capacitor.

Figure 1 Circuit schematic of 2-stage op-amp



The supply voltages V_{DD} and V_{SS}, and drain currents I_5 and I_7 through M5 and M7, respectively, accounts for power dissipation, which is given by:

$$P = (V_{DD} - V_{SS})(I_5 + 2I_7) \tag{10}$$

Area is given by:

$$A = \sum_{i=1}^{n} (W_i * L_i) \tag{11}$$

where W_i is the width and L_i is the length of the i^{th} transistor, respectively, and n is the number of transistors.

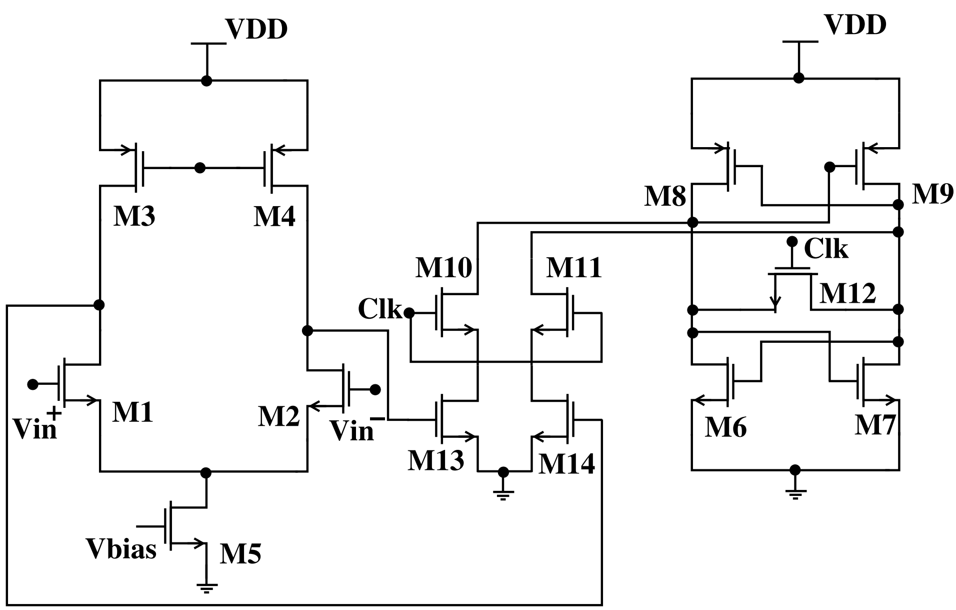
4.2 4-bit flash ADC

In the present-day electronic systems, flash ADC plays a prominent role in converting real-world analogue signal to digital output. In conventional n-bit flash ADC, $2^n - 1$ comparators output the thermometer code by comparing the input voltage simultaneously with reference voltages produced by the resistor ladder circuit. Then the encoder converts the thermometer code into digital output. Flash ADC uses one comparator per quantisation level and 2^n resistors, therefore it has the highest conversion speed than any ADC.

4.2.1 Pseudo-dynamic latched comparator

The pseudo-dynamic latched comparator is designed with a pre-amplifier and a latch (Varghese, 2014). Reset and regeneration are the two operating phases of the latch: In the rest phase, charge imbalance is proportional to the variation in the input signal on the differential nodes of the latch, and in the regeneration phase, the voltage imbalance is amplified to the rail-to-rail logic levels. The schematic of the pseudo-dynamic latched comparator is shown in Figure 2.

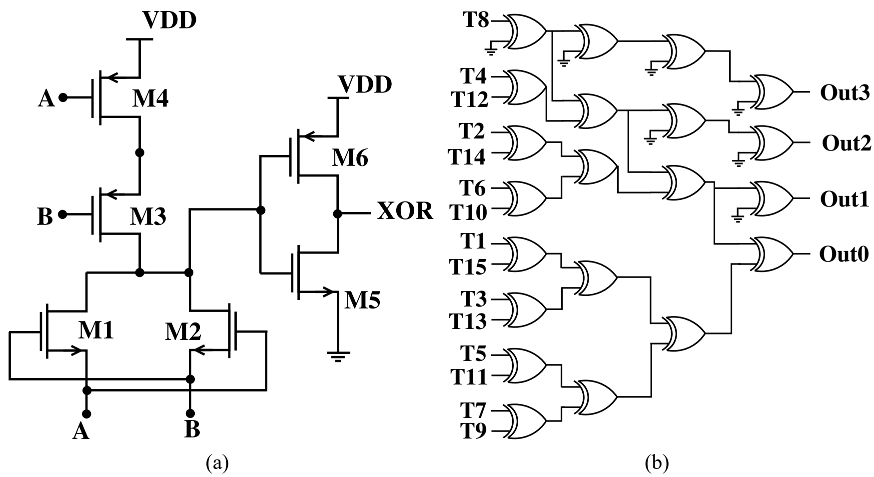
Figure 2 Schematic of pseudo-dynamic latched comparator



4.2.2 Encoder

The output of the comparators is in the form of a thermometer code, which is converted to binary form using full swing XOR Gupta et al. (2020)-based thermometer to binary fat tree encoder (Lee et al., 2002). The schematic of the full swing XOR and block diagram of the fat tree encoder is shown in Figure 3.

Figure 3 Encoder for a thermometer to binary code conversion, (a) schematic of full swing XOR (b) block diagram of the fat-tree encoder



The architecture of the n-bit flash ADC used for design optimisation is shown in Figure 4. Static characteristics of the flash ADC such as *INL* and *DNL*, along with power dissipation (P), are considered for design optimisation (Allen and Holberg, 2002). DNL and INL are given by equations (12) and (13):

$$DNL = \frac{V_{D+1} - V_D}{V_{LSB,Ideal}} - 1; \text{ where } 0 < D < 2^n - 1 \tag{12}$$

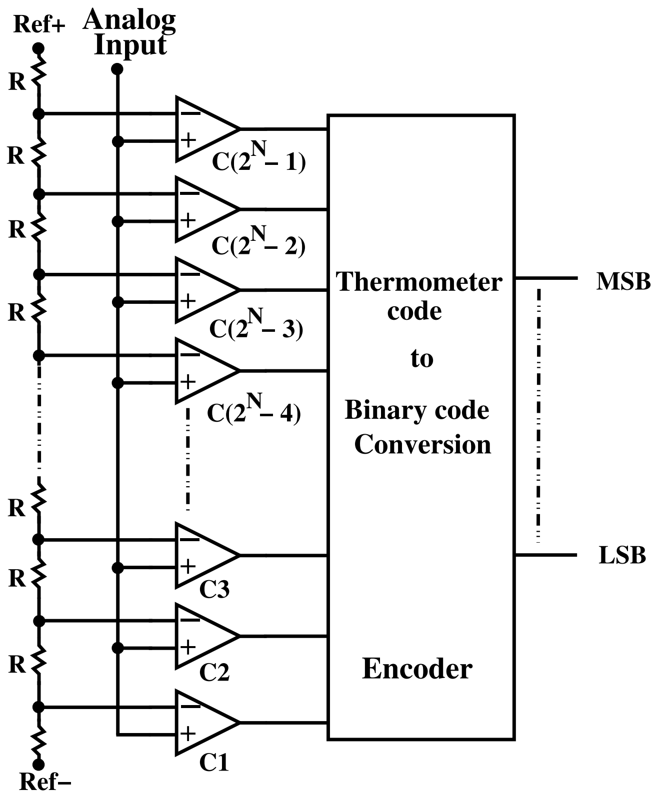
$$INL = \frac{V_D - V_{zero}}{V_{LSB,Ideal}} - D; \text{ where } 0 < D < 2^n - 2 \tag{13}$$

where V_D is the voltage value of the digital output code D, V_{zero} is the voltage value at an all zero output code, $V_{LSB,Ideal}$ is the ideal least significant bit value, and n is the ADC's resolution.

5 PSO-SPICE framework with AWA fitness evaluation for design optimisation

The proposed design automation intends to achieve or outperform the desired specifications of analogue ICs by arriving at the optimum transistor dimensions along with the values of passive elements. The design process is implemented using PSO, and the proposed AWA fitness methodology in MATLAB, and the design solution evolved during each iteration of the optimisation is verified against SPICE simulations seamlessly. The design is carried out using 0.18 μm CMOS technology node, for illustration.

Figure 4 Block diagram of n-bit flash ADC



The design methodology requires two sets of data to progress, the first being the model files of the process node, power supply, and load, the other being design specifications and PSO parameters. The inputs and the outputs of the proposed design methodology to generate optimum design solutions for 2-stage op-amp and 4-bit flash ADC, are as shown in Table 1. The design specifications act as our design objectives and are tabulated in Table 2.

The mandate of the methodology is that the overall design objectives improve the design specifications as much as possible. In 2-stage op-amp, the differential amplifier and current mirror configurations require matching devices in 2-stage op-amp: (M1, M2), (M3, M4), and (M5, M8). Since all comparators must be equal in the ADC, the size of all the MOS devices in the comparators, along with MOS devices in the encoder, are considered as equal. The vector of a possible solution known as particle is as shown in Figure 5.

The methodology is initiated with a set of particles that are generated randomly within a predefined boundary constrained by area specification. Then the corresponding performance metrics are obtained for each of the generated particles through

SPICE simulations. The proposed AWA fitness is then evaluated for PSO generated performance metrics with respect to design specifications. Hereafter, with the inception of PSO, the optimum solution is evolved from the swarm of particles. Thus, the optimisation process calls for data transfer between two platforms, i.e., between PSO and SPICE. This process is automated to support bidirectional data transfer, for multiple iterations, between two platforms using a DOS batch file in a PSO-SPICE framework:

1 Netlist with PSO-MATLAB generated design values [W, L, C_c, and I_b] of 2-stage op-amp and all Ws and all Ls of 4-bit flash ADC, are passed to SPICE

2 SPICE generated circuit performance data in log files are passed to MATLAB for the next PSO iteration.

The PSO-SPICE framework of the proposed methodology using AWA fitness number for analogue circuit design optimisation is as shown in Figure 6.

Table 1 Inputs and outputs of the design methodology

Inputs		*Outputs*	
1	Design specifications: performance metrics as specified by the designer	1	Design solution comprising transistor lengths and widths, passive elements, and/or bias current, etc.
2	Supply voltages and load	2	The circuit is simulated with the optimum design solution to at least match or outperform the desired specifications
3	Process node constants		
4	PSO parameters		

Table 2 Design objectives

	2-stage op-amp	*4-bit flash ADC*
Maximise	*Gain*, *UGBW*, *SR*, and *PM*	
Minimise	*Power* and *area*	*Power*, *DNL*, and *INL*

The PSO process is initiated with a swarm of randomly generated 50 and 30 possible solution vectors of real numbers for a 2-stage op-amp and 4-bit flash ADC, respectively. The PSO parameter of inertia weight is characterised to decrease linearly from 0.9 to 0.4 as the algorithm runs in finding the optimal solution. Initial velocity value of 0.05, and acceleration factors, c_1 and c_2 of 2 and 0.5 are applied to all the particles in the swarm to find an optimal solution. The dimensional range of design parameters [W, L, C_c, and I_b] for generating a swarm of solutions are taken from Harsha and Harish (2018). For practical modelling of layout parasitics for analogue circuits design, the diffusion area and perimeter formed at the source and drain junctions are included and calculated as $ad = as = 2 * W * L_{\min}$ and $pd = ps = 2(W + 2L_{\min})$ (Nagendra, 2018).

For a LTspice netlist, each solution vector is imported seamlessly and simulated. The corresponding performance metrics are extracted from the SPICE waveform data file and log file and transported to the PSO. The PSO carries out the fitness evaluation for each solution in the swarm with respect to target design specifications. The quality of optimisation is enriched by evaluating the fitness of SPICE generated performance metrics directly.

Figure 5 Vector structure of the candidate solution, (a) 2-stage op-amp (b) 4-bit flash ADC

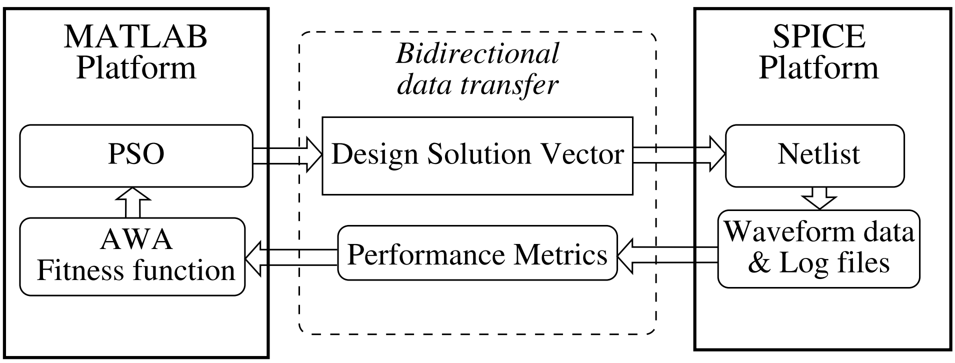
W1	L1	W3	L3	W5	L5	W6	L6	W7	L7	I_b	C_c

(a)

W1	W2	...	W336	L1	L2	...	L336

(b)

Figure 6 PSO-SPICE framework using AWA fitness evaluation for analogue circuit design optimisation



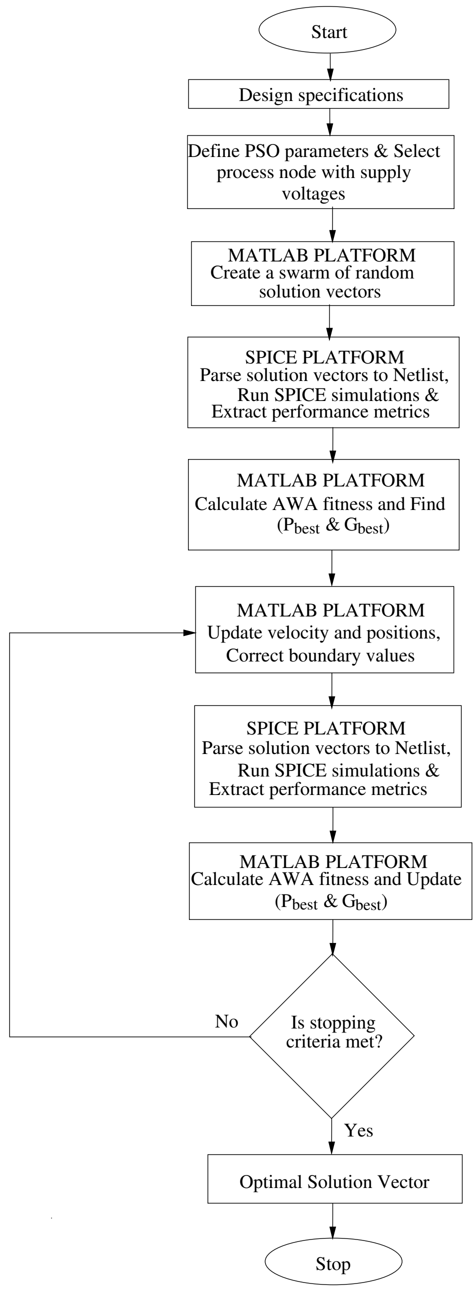
After evaluating the fitness of the initial swarm of solutions, the P_{best} and G_{best} are noted. Then, the velocity and position vectors are updated in accordance with equations (1) and (2), respectively. In the subsequent iterations, as and when the swarm moves away from the search space, the solutions in the swarm are auto-corrected subject to predefined dimensional ranges. Fitness is evaluated for the updated swarm of solutions of any iteration within the range or upon range auto-correction, and the P_{best} and G_{best} are updated if it is superior to previous values. If the G_{best} value changes, the swarm changes its course for the subsequent iteration, thus complying with the principle of stability (Millonas, 1992). This process continues in a loop until the stopping criterion is met. In this work, the maximum number of iterations is selected to be the stopping criterion. Based on the PSO convergence graphs generated from experimental trails, the stopping criterion is selected as 50 iterations for 2-stage op-amp and ten iterations for flash ADC. For iterations more than stopping criterion, it is found that the quality of design solutions is saturated with respect to the desired design. The G_{best} solution obtained at the end is regarded as the optimal solution for a particular design specification. The flowchart of automated analogue design optimisation using AWA fitness driven PSO-SPICE is shown in Figure 7.

6 Results and discussion

6.1 2-stage operational amplifier

The methodology is tested on three different design specifications of 2-stage op-amp, as mentioned in Tables 3 and 4. While results 3 and 4 represent the optimal solution obtained using PSO with the Yu and Mao (2009) fitness function, results 5 and 6 represent the optimal solution obtained using PSO with the SP fitness function (Papadopoulos et al., 2000). Results 7, 10, and 13 are the optimal solutions obtained using PSO with the proposed AWA fitness evaluation methodology.

Figure 7 Flowchart of automated analogue design optimisation using AWA fitness driven PSO-SPICE



The Yu fitness and SP fitness methodologies suffer from the possibility of significantly different design solutions depending on the quality of randomly generated swarms of initial solutions. However, the AWA fitness evaluation decouples the design solution from the quality of the initial solution and generates global optimum solutions, i.e., optimisation of all performance metrics. The area of the design is computed as the area of all transistors only, with interconnects excluded. For 2-stage op-amp, the corresponding PSO convergence is shown in Figure 8 and the behaviour of performance metrics in Figure 9.

Table 3 2-stage op-amp's performance metrics obtained using PSO and fitness functions for the design 1 of specifications of MOGA

Performance metrics	*Design 1*	*MOGA*	*CRPSO*	*PSO + Yu fitness*	*PSO + Yu fitness*	*PSO + SP fitness*	*PSO + SP fitness*	*PSO + AWA fitness*
		Result 1	*Result 2*	*Result 3*	*Result 4*	*Result 5*	*Result 6*	*Result 7*
Gain (dB)	70	76	65.47	0.54	73.47	66.11	64.18	70.04
UGBW (MHz)	1.5	1.5	22.57	0.01	11.12	99.99	100	17.63
PM (°)	60	70	64.59	159.96	74.46	16.84	42.46	60.01
SR (V/μs)	1.5	2.25	25.09	8.87	11.26	109.31	108	27.79
Power (mW)	0.1	0.04	0.45	0.20	0.21	0.2	0.40	0.09
Area (μ m^2)	200	559	196	132.43	138.75	308	178.78	108.00
Time (s)	-	-	6,162	5,799	6,238	6,276	4,306	3,844

Source: Dendouga et al. (2014) and Harsha and Harish (2018)

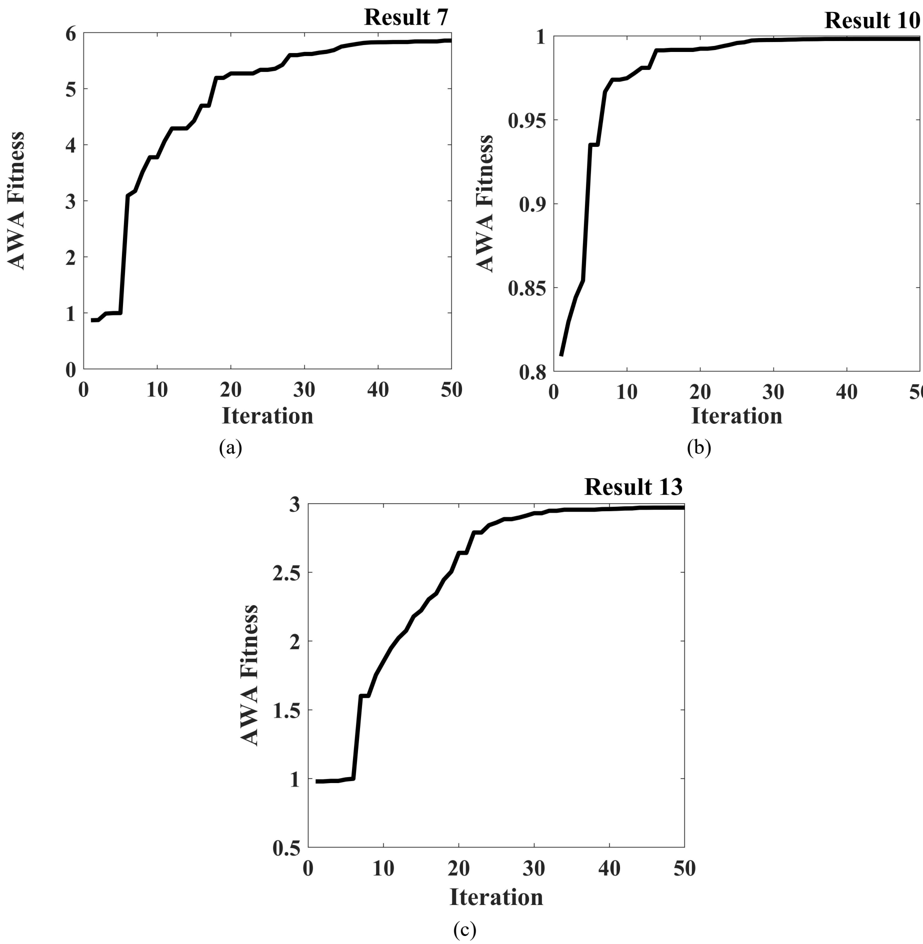
Table 4 2-stage op-amp's performance metrics obtained using PSO and fitness functions for proposed designs 2 and 3

Performance metrics	*Design 2*	*MOGA*	*CRPSO*	*PSO + AWA fitness*	*Design 3*	*MOGA*	*CRPSO*	*PSO + AWA fitness*
		Result 8	*Result 9*	*Result 10*		*Result 11*	*Result 12*	*Result 13*
Gain (dB)	80	74.8	63.47	79.56	70	68.37	69.3	72.1
UGBW (MHz)	5	7.32	8.042	18.29	5	8.36	9.17	45.96
PM (°)	70	76.1	72.25	73.00	70	70.63	78.26	70.00
SR (V/μs)	10	7.41	11.91	12.54	10	10.01	6.14	44.56
Power (mW)	0.5	0.39	0.18	0.33	0.5	0.57	0.23	0.49
Area (μ m^2)	100	254	54.6	99.67	100	634	61.5	87.85
Time (s)	-	5,879	5,615	3,836	-	6,112	6,013	4,249

The PSO results obtained using Yu fitness are stuck at a local optima, due to the adaptive weights associated with the Yu fitness function, indicating less number of performance metrics being optimised. This degrades the efficiency of the multi-parameter optimisation due to the epistatic nature of the objectives over successive iterations.

Equivalently, the SP fitness stumbles by virtue of acceptable ranges and change in swarm behaviour. Here, the fitness function determines the errors of the solution vector with respect to the design specification and its acceptable range. With multi-objective optimisation, the cumulative square of positive and negative errors results in a high fitness value, but yet a suboptimal solution. Because in this case, the G_{best} updates and in turn the position of the swarm of solutions changes, but there is a likelihood of imitating the errors of the previous iteration, thereby it ends at a suboptimal solution, where only a few objectives are achieved.

Figure 8 PSO convergence for AWA fitness driven PSO optimisation of 2-stage op-amp, (a) design 1 (b) design 2 (c) design 3

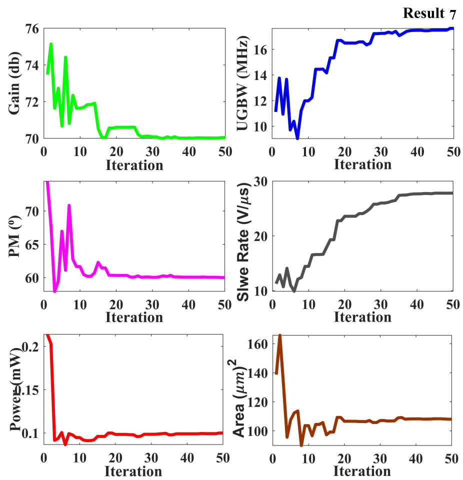


The performance metrics of 2-stage op-amp of the proposed AWA fitness driven PSO are compared with Yu fitness driven PSO, SP fitness driven PSO, multi-objective genetic algorithm (MOGA) (Dendouga et al., 2014) and craziness-based PSO (De et al., 2017) for design 1 specifications and the results are tabulated in Table 3. The result 7 of the AWA fitness driven PSO demonstrate the accuracy and even betterment of design specifications for each performance metric, resulting in best optimal design solution. For design 1, while open-loop DC gain, PM and power dissipation are accurate, UGBW, SR and area are significantly better than specifications.

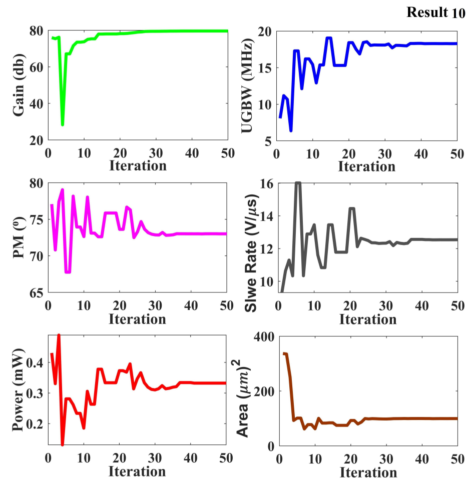
Table 5 Design parameters of results 1 to 13 of 2-stage op-amp

Transistor parameters (μm)	*Result 1*	*Result 2*	*Result 3*	*Result 4*	*Result 5*	*Result 6*	*Result 7*	*Result 8*	*Result 9*	*Result 10*	*Result 11*	*Result 12*	*Result 13*
W1 = W2	1.34	11.4	1.00	3.8387	12.0	11.9913	1.7623	2.23	2.43	11.9949	8.82	10.84	5.6953
L1 = L2	1.5	1.8	1.1030	0.9238	0.18	0.18377	0.9969	0.558	1.07	0.7485	1.66	0.771	0.6787
W3 = W4	8.5	14.2	4.2010	17.6779	17.1870	28.00	19.0897	10.4	9.33	12.7579	26.9	11.2	7.5601
L3 = L4	1.11	0.818	1.6399	0.6572	0.61176	0.1801	0.4284	1.77	0.763	0.9580	1.87	0.886	0.3943
W5 = W8	1.4, 23.5	9.9	11.9037	15.3260	24.00	22.5631	23.5556	8.8	13.9	2.1631	20.6	5.17	15.1792
L5 = L8	0.44, 0.68	0.422	1.0217	1.4744	0.18	0.18	1.5226	0.608	0.445	1.0408	1.74	0.316	1.9505
W6	48	254.9	308.143	104.732	32.00	209.625	53.6922	33.9	38.6	64.0854	353	59.3	87.9486
L6	0.92	0.318	0.2597	0.3937	0.18	0.18	0.18	0.315	0.549	0.1811	0.984	0.191	0.1896
W7	6	85.5	41.7424	53.9962	135.557	147.148	34.4590	135	24.8	24.1644	119.8	19.1	50.6861
L7	0.8	0.298	0.5545	0.7601	2.00	0.8175	1.1852	1.46	0.211	1.4249	0.886	0.181	0.4737
I_b (μA)	-	13.7	16.12	18.48	30.00	30.00	18.31	19.7	22.9	19.02	25.9	12.7	26.91
C_c (pF)	-	0.63	1.9271	1.7401	0.44	0.44	0.6980	2.89	2.14	1.5628	2.72	2.47	0.6261

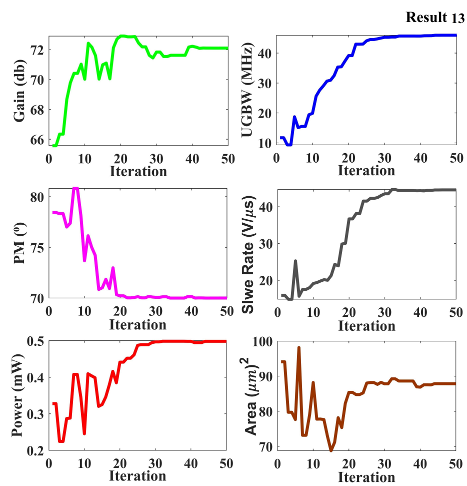
Figure 9 Behaviour of performance metrics – open-loop DC gain, UGBW, PM, SR, power dissipation and Area for AWA driven PSO optimisation of 2-stage op-amp, (a) design 1 (b) design 2 (c) design 3 (see online version for colours)



(a)



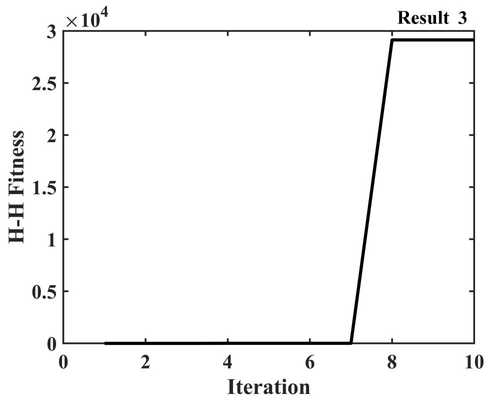
(b)



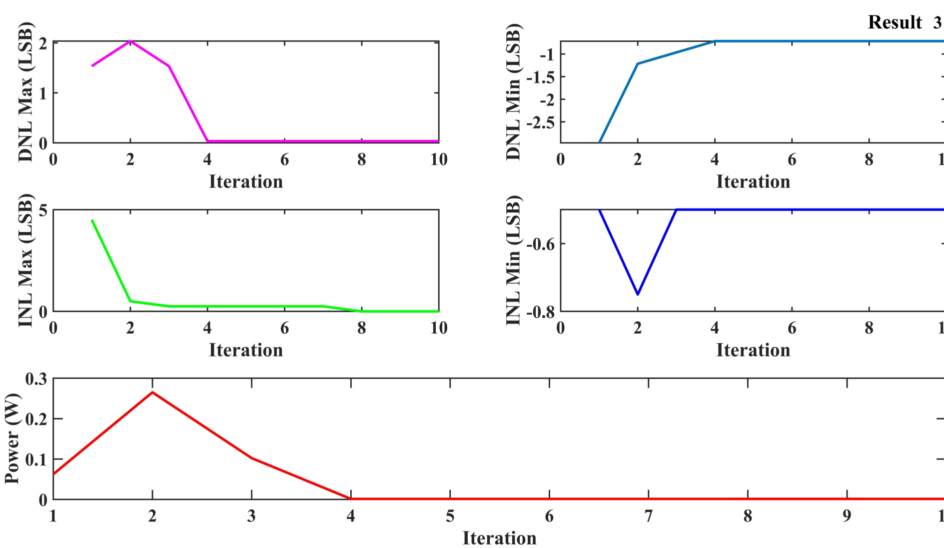
(c)

The quality of the design in case of Yu fitness driven PSO and SP fitness driven PSO has a strong dependence on the initial solution and adaptive weights, respectively as indicated by results 3 to 6 of Table 3. In contrast, the AWA fitness is directly evaluated with respect to the desired target, and it is independent of acceptable target range and does not require any adaptive weights. The deployment of AWA fitness evaluation enables unique optimal solution for a particular design specification that is generated independent of the initial random solution and the iteration count, when the iteration count is above a minimum. The corresponding results are demonstrated for different set of specifications designs 2 and 3, as shown in Table 4. The range of design outperformance, against given specifications, with the proposed methodology varied between –0.55% to 3% for gain, 365% to 1,175% for UGBW, 0% to 4.2% for PM, 25% to 1,852% for SR, 2% to 34% for power and 0.33% to 46% for area, for designs 1, 2 and 3. The corresponding behaviour of PSO convergence and convergence of its performance metrics using AWA fitness driven PSO optimisation are shown in Figures 8(a), 8(b), 8(c), 9(a), 9(b) and 9(c), respectively. It can be seen that all performance metrics are optimised requiring 50 iterations. For 2-stage op-amp, the corresponding final optimal design parameters of W, L, C_c, and I_b generated are tabulated in Table 5.

Figure 10 AWA fitness driven PSO optimisation of 4-bit flash ADC, (a) PSO fitness convergence (b) behaviour of performance metrics – DNL, INL and power dissipation (see online version for colours)



(a)



(b)

6.2 4-bit flash ADC

To demonstrate the efficacy of the proposed methodology across mixed-signal circuits of varying complexity, it is tested on 4-bit flash ADC for the given design specifications and its performance metrics obtained using PSO and various fitness functions are tabulated in Table 6. While result 1 represents the optimal solution obtained using PSO with the Yu and Mao (2009) fitness function, result 2 represents the optimal solution obtained using PSO with the SP fitness function (Papadopoulos et al., 2000). The result 3 is the optimal solution obtained using PSO with the proposed AWA fitness evaluation methodology. The design outperformance, with respect to given specifications, is observed on all five performance metrics: power of 28.5%, DNL maximum of 100%, DNL minimum of 46%, INL maximum of 96.5% and INL minimum of 20.6%. It is demonstrated that the AWA fitness evaluation decouples the design solution from the quality of the initial solution. Hence, the deployment of AWA fitness evaluation enables a unique optimal solution for a given design specification that is generated independent of the initial random solution and the iteration count, when the iteration count is large enough. Further, AWA fitness function assists in finding an optimal design solution even with a wide range of W and L, unlike a narrow range of W and L required by the Yu and SP fitness functions.

For the 4-bit flash ADC, the behaviour of PSO convergence and performance metrics using AWA fitness are shown in Figure 10. The transistor parameters of the 4-bit flash ADC design for results 1, 2 and 3 are tabulated in Table 7. It may be noted that the area of the design is computed as the area of all transistors only, with interconnects excluded.

Table 6 Performance metrics of 4-bit flash ADC obtained using PSO and various fitness functions

Performance metrics	*Design specifications*	*PSO + Yu fitness*	*PSO + SP fitness*	*PSO + AWA fitness*
		Result 1	*Result 2*	*Result 3*
Power dissipation (mW)	2	1.25	0.771	1.43
DNL maximum (LSB)	1	0.25	0.25	0
DNL minimum (LSB)	–0.9	–0.49	–1	–0.49
INL maximum (LSB)	1	0.285	1.78	0.035
INL minimum (LSB)	–0.9	–0.714	–0.464	–0.714
Time (s)		5,888	4,390	5,968
Area (μ m^2)		11.84	22.07	10.88

Table 7 Transistor parameters of the 4-bit flash ADC design for results 1, 2 and 3

Transistor parameters (μ m)	*Result 1*	*Result 2*	*Result 3*
For all W	0.18	0.219	0.18
For all L	0.1958	0.3	0.18

7 Conclusions

An integrated AWA fitness function driven PSO-SPICE framework, with simple, automated, and seamless bidirectional interfaces for multi-objective optimisation of analogue and mixed-signal integrated circuits, is presented. The proposed methodology addresses the design complexity and scalability by optimising 2-stage op-amp and 4-bit flash ADC, respectively. The design of a 2-stage op-amp having eight transistors with 12 design parameters and 4-bit flash ADC having 336 identical transistors with four design parameters are efficiently automated for design optimisation to achieve respective design specifications. The efficacy of a novel AWA fitness evaluation function for PSO technique is compared against Yu fitness and SP fitness functions and shown to excel the design specifications, besides being simple and requiring low computational cost. The AWA fitness is directly evaluated with respect to the desired target, and it is independent of the acceptable target range and does not require any adaptive weights. The AWA fitness evaluation enables a unique optimal solution that is generated independent of the quality of the initial solution, the iteration count and without the need for applying adaptive weights. As AWA fitness evaluation is based on design optimality and not on distance measure, large design outperformance is recognised, facilitating large design outperformance. The design solutions generated by AWA fitness driven PSO are compared and found to be superior to MOGA and CRPSO work. The range of design outperformance against given specifications of 2-stage op-amp with the proposed methodology varied between –0.55% to 3% for gain, 365% to 1,175% for UGBW, 0% to 4.2% for PM, 25% to 1,852% for SR, 2% to 34% for power and 0.33% to 46% for area, for designs 1, 2 and 3. The design outperformance of 4-bit flash ADC against given specifications is observed on all five performance metrics: power of 28.5%, DNL maximum of 100%, DNL minimum of 46%, INL maximum of 96.5% and INL minimum of 20.6%. The quality of the design optimisation is enhanced by directly measuring the fitness on SPICE generated data in each iteration, which is facilitated by the proposed integrated PSO-SPICE framework. Thus, the AWA fitness function driven PSO optimisation methodology implemented in an integrated PSO-SPICE framework, exemplies a robust, scalable, and precise method for multi-objective optimisation of analogue and mixed-signal circuits of varying scale and design complexity. Further, the AWA fitness methodology is generic in nature and can be applied to determine the best optimal solution, where its optimality rather than distance-based closeness with respect to the desired solution is the requirement, over all application domains.

References

Allen, P.E. and Holberg, D.R. (2002) *CMOS Analog Circuit Design*, 2nd ed., Oxford University Press, New York.

Bansal, S., Ghaderi, E., Puglisi, C. and Gupta, S. (2021) 'Neural-network based self-initializing algorithm for multi-parameter optimization of high-speed ADCs', *IEEE Transactions on Circuits and Systems-II: Express Briefs*, Vol. 68, No. 1, pp.106–110.

De, B.P., Maji, K.B., Kar, R., Mandal, D. and Goshal, S.P. (2017) 'Application of improved PSO for optimal design of CMOS two-stage op-amp using nulling resistor compensation circuit', *Proceedings of 2017 Devices for Integrated Circuit (DevIC)*, India.

Deb, K. and Padhye, N. (2014) 'Enhancing performance of particle swarm optimization through an algorithmic link with genetic algorithms', *Computational Optimization and Applications*, Vol. 57, No. 2, pp.761–794.

Dendouga, A., Oussalah, S., Thienpont, D. and Lounis, A. (2014) 'Multiobjective genetic algorithms program for the optimization of an OTA for front-end electronics', *Advances in Electrical Engineering*, No. 1, pp.1–5.

Fakhfakh, M., Cooren, Y., Sallem, A., Loulou, M. and Siarry, P. (2010) 'Analog circuit design optimization through the particle swarm optimization technique', *Analog Integrated Circuits and Signal Processing*, Vol. 63, No. 1, pp.71–82.

Garbaya, A., Kotti, M., Drira, N., Fakhfakh, M., Tlelo-Cuautle, E. and Siarry, P. (2018) 'An RBF-PSO technique for the rapid optimization of CMOS analog circuits', *7th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, pp.1–4.

Gomes de Almeida, B.S. and Leite, V.C. (2019) *Chapter 3: Particle Swarm Optimization: A Powerful Technique for Solving Engineering Problems, Swarm Intelligence*, IntechOpen Publisher.

Gonzalez-Echevarraa, R., Roca, E., Castro-Lopez, R., Fernandez, F.V., Sieiro, J., Lopez-Villegas, J.M. and Vidal, N. (2017) 'An automated design methodology of RF circuits by using pareto-optimal fronts of EM-simulated inductors', *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 36, No. 1, pp.15–26.

Gupta, M., Pandey, B.P. and Chauhan, R.K. (2020) 'CMOS-based XOR gate design for full swing output voltage and minimum power delay product', *Proceedings of Intelligent Computing and Communication (ICICC)*, Springer, India, pp.99–107.

Harsha, M.V. and Harish, B.P. (2018) 'An integrated maxfit genetic algorithm-SPICE framework for 2-stage op-amp design automation', *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Hong Kong, pp.170–174.

Harsha, M.V. and Harish, B.P. (2020) 'Artificial neural network model for design optimization of 2-stage op-amp', *24th International Symposium on VLSI Design and Test (VDAT)*, IIT, Bhubaneswar, India.

Kennedy, J. and Eberhart, R. (1995) 'Particle swarm optimization', *Proceedings of ICNN'95 – International Conference on Neural Networks*, Australia, pp.1942–1948.

Lee, D., Yoo, J., Choi, K. and Ghaznavi, J. (2002) 'Fat tree encoder design for ultra-high speed ash A/D converters', *The 2002 45th Midwest Symposium on Circuits and Systems (MWSCAS-2002)*, USA, Vol. 2, pp.87–90.

Lourenco, N., Rosa, J., Martins, R., Aidos, H., Canelas, A., Povoa, R. and Horta, N. (2018) 'On the exploration of promising analog IC designs via artificial neural networks', *Proceedings of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, Czech Republic, pp.133–136.

Lyu, W., Xue, P., Yang, F., Yan, C., Hong, Z., Zeng, X. and Zhou, D. (2018) 'An efficient Bayesian optimization approach for automated optimization of analog circuits', *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 65, No. 6, pp.1954–1967.

Mallick, S., Kar, R., Mandal, D. and Ghoshal, S.P. (2017) 'Optimal sizing of CMOS analog circuits using gravitational search algorithm with particle swarm optimization', *International Journal of Machine Learnning and Cybernetics*, Vol. 8, No. 1, pp.309–331.

Millonas, M.M. (1992) 'Swarms, phase transitions, and collective intelligence', *Proceedings of the Artificial Life Conference*.

Nagendra (2018) [online] http://www.ee.iitm.ac.in/nagendra/cadinfo.html (accessed 26 March 2020).

Papadopoulos, S., Mack, R.J. and Massara, R.E. (2000) 'A hybrid genetic algorithm method for optimizing analog circuits', *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (Cat. No. CH37144)*, USA, Vol. 1, pp.140–143.

Ratan, S., Mondal, D., Anima, R., Kumar, C., Kumar, A. and Kar, R. (2016) 'Area optimization of two-stage amplifier using modified particle swarm optimization algorithm', *2016 International Conference on Advances in Computing, Communications and Informatics (ICACCI)*, India, pp.230–235.

Sumalya, G., Bishnu, P.D., Rajib, K., Mandal, D. and Kumar, M.A. (2019) 'Optimal design of complementary metal-oxide-semiconductor analogue circuits: an evolutionary approach', *Computers and Electrical Engineering*, Vol. 80, pp.1–19.

Tlelo-Cuautle, E. and Sanabria-Borbon, A. (2016) 'Optimising operational amplifiers by evolutionary algorithms and GM/ID method', *International Journal of Electronics*, Vol. 103, No. 10, pp.1665–1684.

Varghese, G.T. (2014) *Design and Implementation of a Novel Ash ADC for Ultra Wide Band Applications*, PhD thesis, Indian Institute of Technology, Rourkela, India.

Yu, J. and Mao, Z. (2009) 'A design method in CMOS operational amplifier optimization based on adaptive genetic algorithm', *WSEAS Transactions on Circuits and Systems*, Vol. 8, No. 7, pp.548–558.