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## Cascaded controller for single-phase shunt active power filter and STATCOM

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**Abstract:** Reactive power and harmonic current compensation are considered as two important issues in the electrical power system since they have strong impact on real power loss, voltage stability, resonance and operation cost. This paper presents a simple, yet effective cascade controller which is analysed and implemented on a single-phase grid-connected H-bridge and multilevel U-cell inverters. The proposed controller is used for the single-phase STATCOM and shunt active power filter. The DC bus capacitor voltages are regulated with the proportional-integral (PI) controllers. The proportional resonant (PR) controller is used for AC current control. The cascade operation of the PI and the PR controllers generates the control signal for the sinusoidal pulse width modulation. The reactive power compensation and harmonic current elimination are carried out by using the fundamental component of the grid current. The performance of the controller is analysed and the results of simulation and experimental work are presented.

**Keywords:** power quality; single-phase STATCOM; shunt active power filter; SAPF; current controller.

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## 1 Introduction

Reactive power and harmonic current compensation are considered as two important issues in the electrical power system since they have the strong impact on real power loss, voltage stability, resonance and operation cost. The shunt reactors, capacitor banks and passive harmonic filters in the electrical power system were the traditional solutions to these problems. However, the performance of these passive elements is highly affected by the grid impedance and load variations. These passive elements may cause resonance in the system or fail to respond properly to many rapidly changing dynamic loads (Sharifabadi et al., 2016; Dixon et al., 2005). Meanwhile, increasing nonlinear components in the network such as power electronic devices and drive circuits in energy conversion have increased the total harmonic distortion (THD) in supply currents (Khadkikar, 2012). Moreover, the advancement and deployment of distributed and renewable energy resources, which are mostly power electronic converter interfaced resources, has added another level of the complexity to the problem (Parthasarathy et al., 2019; Akkala et al., 2019). In some cases, installation of renewable energy systems is accompanied by a reactive power or harmonic compensator to meet the grid requirements

(Fuad et al., 2020). The advanced technology used for reactive power compensation and harmonic current elimination contains the three-phase or single-phase DC/AC converters (inverters). The shunt-connected converters to the load at the point of common coupling (PCC) are controlled in order to generate or absorb the reactive power of the load (Gültekin and Ermis, 2013; Singh et al., 2009; Latran et al., 2015). The shunt active power filters (SAPFs) are also designed with the same structure of inverters in order to inject the harmonic currents demanded by the nonlinear loads (Malinowski et al., 2010). The SAPFs and static synchronous compensator (STATCOM) show fast response and meritorious performance during reactive power compensation and harmonic current elimination. The extraction of harmonic and reactive current components is a vital signal processing part of the SAPF and STATCOM, because it has a strong impact on response time of current controller, number of sensors used for voltage and current measurements, and the complexity of the control algorithm. The unbalance and single-phase operations are also demanded due to the nature of the industrial loads (Xu et al., 2010) and renewable power generation systems like the photovoltaic systems and wind energy conversion system (Varma et al., 2015).

Although many control methods have been implemented, some of those do not fulfil the IEEE Standard 1459-2010 requirements under highly distorted source voltage and three-phase unbalanced operations (Vardar et al., 2009). The hysteresis current controller and the proportional-integral (PI) regulator have been frequently implemented on the control of inverters. The hysteresis controller is robust and keeps the actual current in a constant hysteresis band with varying switching frequency. Its performance depends on the loading conditions and switching frequency (Vardar and Akpınar, 2011). Although adaptive hysteresis band with constant switching frequency techniques have been developed however, generally speaking, varying switching frequency is the major drawback of this control method (Dos Santos and Da Silva, 2014). In three-phase systems, the synchronously rotating reference frame at the fundamental frequency is usually selected to operate the PI controllers under DC signals (Sing et al., 2011). Due to the specific control bandwidth, the PI controller has a limited success on harmonic current elimination. An alternative current controller was designed by using the PI regulator and series of resonant controllers (vector PI controllers) simultaneously for pre-specified current harmonics (Trinh and Lee, 2013; Yi et al., 2014). The frequency spectrum of the load current harmonics changes in time due to the variation of nonlinear loads. Hence, the effective controller logic for the reactive power compensation and current harmonics elimination can be designed by processing the fundamental component of the current at the power frequency in the controller instead of using series resonant controllers.

Recently, advanced control methods such as sliding mode control and neural network aided control techniques are proposed for reactive and harmonic current compensation (Fei and Wang, 2019; Fei and Chen, 2020). Model-based and model predictive control (MPC) methods have been proposed and proved their merits for reactive power and current harmonic mitigation (Tarisciotti, 2017; Ferreira et al., 2018). However, the complexity of design and implementation limits is the main drawbacks of these control techniques. Considering ever-increasing complexity of electric power system, converter topologies and type of loads, need for a generic, simple, easily applicable, and yet effective control method is crucial in this field.

A novel cascade controller has been proposed and implemented in simulation environment in Hafezi et al. (2014). The proposed controller tracks the fundamental

component of supply current by employing a cascade outer PI and a single inner proportional resonant (PR) controller (Hu et al., 2009; Zmood and Holmes, 2003). The inner PR controller works with a feedback of error between the actual and reference grid currents. The reference grid current is generated from the fundamental component of grid voltage and the resonance frequency of the PR is set to the fundamental frequency of the grid voltage. The reference signal at the output of the PR is generated at the grid voltage frequency for the PWM module. The compensation of time delay which is a significant parameter in digital controllers can also be ignored at this low-frequency operation at 50–60 Hz (Trinh and Lee, 2013).

The previously proposed current controller in Hafezi et al. (2014) has been improved and implemented on two different single-phase inverters in this paper. In particular, the paper provides experimental results for full H-bridge single-phase converter with bipolar switching strategy that is widely used in photovoltaic systems. The common-mode voltage is DC voltage hence the common-mode current is negligible even if it is connected to the grid without the isolation transformer (Gonzalez et al., 2007). Moreover, the proposed control method is expanded to be used in cross-connected U-cell multilevel converter with reduced number of switches. A five-level output voltage is generated by using six semiconductors in the SAPF and STATCOM application (Balikci and Akpinar, 2014). The higher-level output voltage waveform such as the seven-level output voltage can also be generated by adding one more cell unit (Kangarlu and Babaei, 2013). The other convenient U-cell topologies are also available with unequal DC voltage levels across the capacitors (Sanjeevan et al., 2015; Vahadi et al., 2016). Therefore, the results and findings of the paper prove that the proposed cascade current controller can be easily implemented in different converter structure with minor modification. There are many multilevel converter topologies that suitable for the implementation of the proposed current controller (Das et al., 2020; Bhat et al., 2017; Annamalai and Udhayakumar, 2019).

The remaining part of the paper is organised as follows: a model of single-phase H-bridge converter and the proposed cascaded control block diagram for H-bridge converter are presented in Section 2. Section 3 presents the model of U-cell multilevel converter with current harmonic elimination and reactive power compensation. The results of simulation and experimental work are given and elaborated in Section 4. Finally, the conclusions have been pointed out in Section 5.

## 2 H-bridge converter with proposed controller

The electrical circuit of a single-phase SAPF and STATCOM with H-bridge voltage source inverter (VSI) topology together with proposed controller is shown in Figure 1. Detailed modelling of H-bridge converter with proposed current controller is presented in Hafezi et al. (2014) where the proposed controller has been examined as single-phase STATCOM with linear load only by simulation study. Here, the proposed controller is updated so its functionality is extended for SAPF and STATCOM with linear and nonlinear loads, moreover, experimental results are also provided. The state-space model of the single-phase VSI converter is given as equation (1) where  $v_s$  is the grid side AC voltage,  $x_1$  is converter current ( $I_C$ ),  $x_2$  is DC bus capacitor voltage ( $V_{DC}$ ) and  $x_3$  is the converter output voltage.  $S_1$  and  $S_2$  are complimentary switching functions as defined in Hafezi et al. (2014).

$$\begin{cases} \frac{dx_1}{dt} = -\frac{R}{L}x_1 - \frac{1}{L}x_2 + \frac{2S_2}{L}x_2 + \frac{1}{L}v_s \\ \frac{dx_2}{dt} = \frac{1-2S_2}{C}x_1 \\ x_3 = (1-2S_2)x_2 \\ y = x_1 \end{cases} \quad (1)$$

DC bus voltage ( $V_{DC}$ ) control, which is the outer control loop, plays an important role in the proposed controller. The output of PI estimates the magnitude of source current which has been used as magnitude of source current reference. The PI output is multiplied with the normalised grid voltage ( $V_{s,pu}$ ), for unity power factor operation. Here,  $V_{s,pu}$  is received from the phase-locked loop (PLL) block which tracks the fundamental component of the voltage. The multiplication of PI output with  $V_{s,pu}$  gives the source current reference signal ( $i_s^*$ ). The difference between  $i_s^*$  and  $i_s$  measurement that is the error signal is fed through the PR controller.  $i_s$  measurement can be obtained from the summation of  $I_C$  and  $I_L$  as it is proposed in Hafezi et al. (2014), however here instead of two current measurements (current sensors), only the grid current measurement ( $i_s$ ) is used in control loop. The output of the PR controller is assigned as the control signal ( $v_c^*$ ) of converter and it passed through the sinusoidal pulse width modulation (SPWM) block which generates gate signals to run H-bridge VSI switches. The proposed control method ensures that H-bridge converter injects only reactive power and distortion power required by the load so that only pure active power will be supplied from the source.

The reference ( $i_s^*$ ) and actual ( $i_s$ ) currents are the AC currents therefore, their phase and magnitude can be tracked by the PR controller without time delay. The block diagram, transfer function and controller gains design procedure are explained in Hafezi et al. (2014) and have been avoided here for brevity.

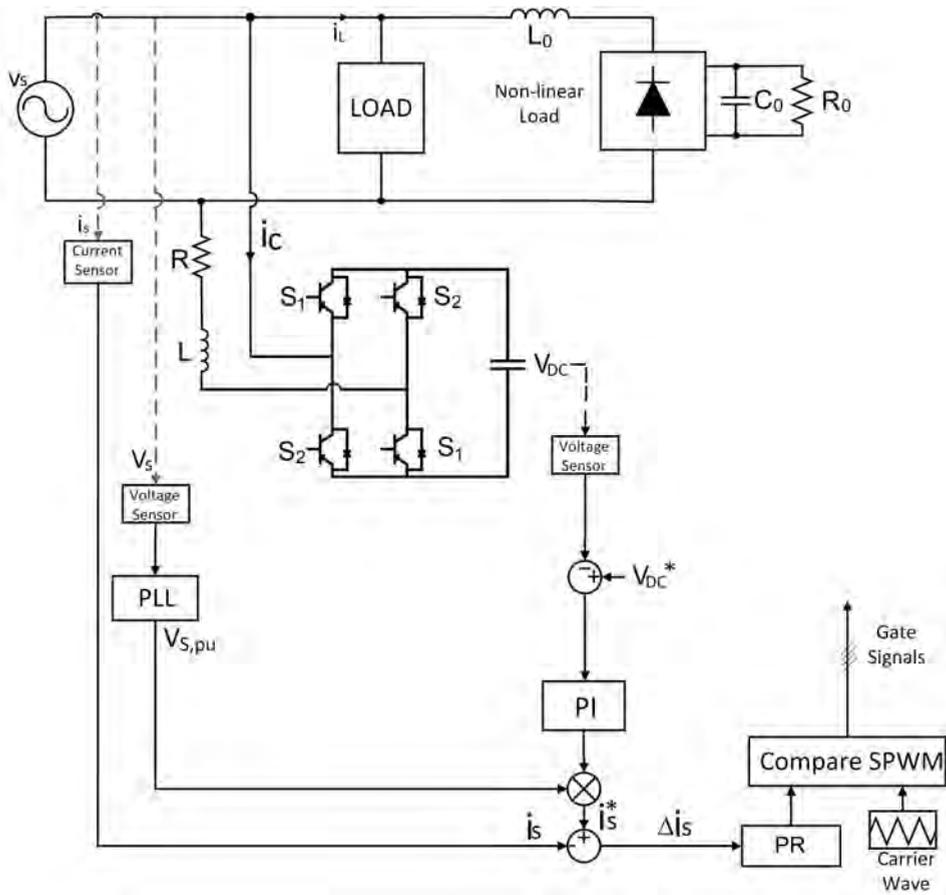
The fundamental component of this control voltage ( $v_c^*$ ) is expected to have phase shift (power angle) with respect to the grid voltage to control the real power flow demanded by the load.

$$v_c^* = V_c \sin(\omega t - \delta) \quad (2)$$

where  $V_c$  is defined as magnitude and  $\delta$  is the phase shift (power angle) of the control voltage with respect to the source voltage. It has been shown that by properly controlling the magnitude and phase angle of the control voltage, the reactive power and active power flow through the converter can be effectively controlled.

The power converter of the SAPF and STATCOM is a boost-type converter. The DC link voltage value and its variation affect the magnitude of the control voltage  $V_c$  and its phase displacement  $\delta$  (Hafezi et al., 2014). The controller can demand some amount of real power from the grid to compensate the converter losses and regulate the DC bus voltage. This real power flow is controlled by the value of  $\delta$ , while the distortion and reactive power flow are basically controlled by the magnitude of control voltage  $V_c$ . The design of the PI controller is carried out by considering the stabilisation of the DC link voltage under these constraints.

**Figure 1** Single-phase SAPF and STATCOM with H-bridge converter

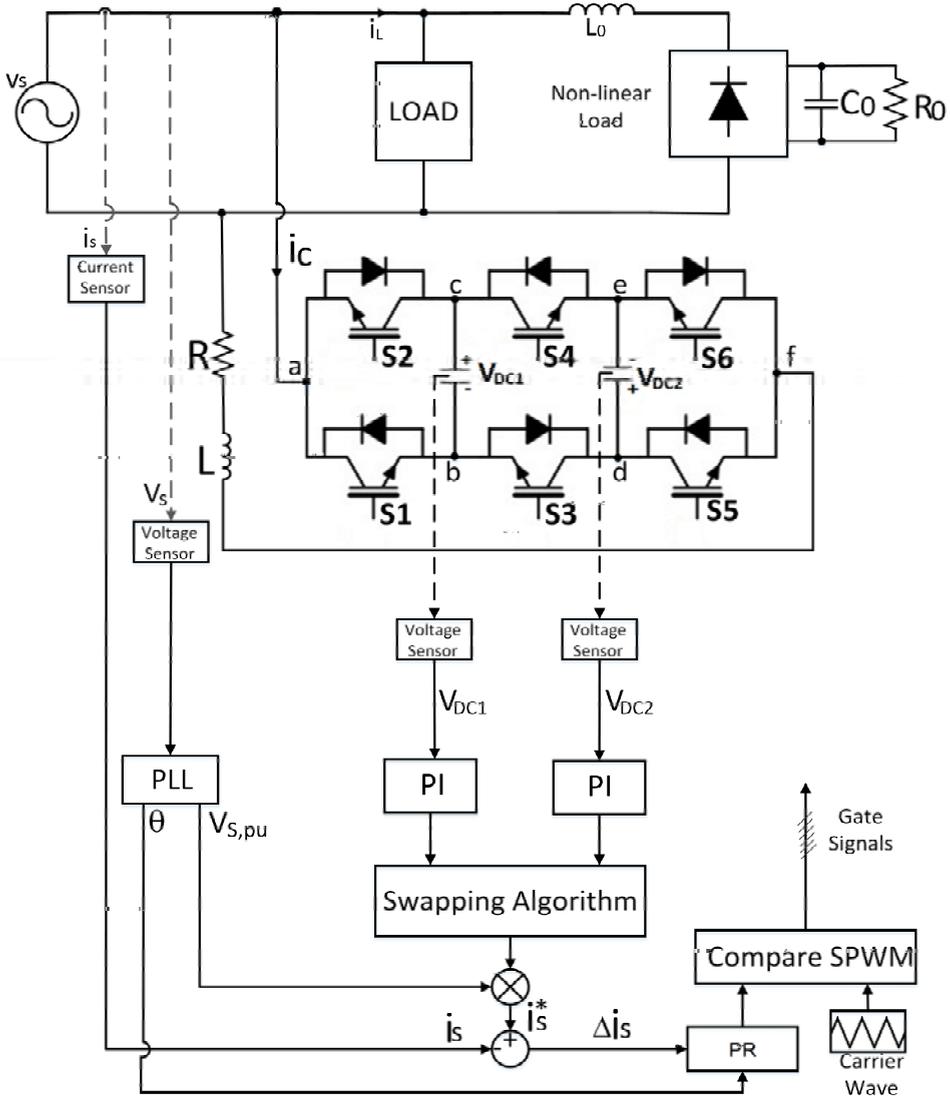


Source: Hafezi et al. (2014)

### 3 Multilevel converter with proposed controller

A single-phase cross-connected U-cell converter topology depicted in Figure 2, which has six semiconductor switches and two DC link capacitors. This converter does not have a common DC link which is usually required for inverter operation in motor drives, but its multilevel structure has the capability of reactive power control in either direction. The switching states of U-cell converter ( $S_1, S_3$  and  $S_5$ ) are given in Table 1. The switches ( $S_1, S_2$ ), ( $S_3, S_4$ ), and ( $S_5, S_6$ ) work in complementary, therefore the standard PWM ports of the digital signal processor (DSP) and all its technical features can be implemented to control the gate drive circuits of IGBTs.

**Figure 2** Single-phase SAPF and STATCOM with multilevel converter



**Table 1** Switching states of U-cell converter

Output voltage	$S_1$	$S_3$	$S_5$
$2V_{dc}$	0	1	0
$V_{dc}$	0	1	1
0	1	1	1
$-V_{dc}$	1	0	0
$-2V_{dc}$	1	1	0

### 3.1 Multilevel converter model

The converter terminal voltage ( $V_{af}$ ) at the grid side is equal to the sum of the potential differences  $V_{ab}$ ,  $V_{bd}$  and  $V_{df}$  as it is written below.

$$V_{af} = V_{ab} + V_{bd} + V_{df} \quad (3)$$

where the sub-terminal voltages given below can be obtained from the DC capacitor voltages and switching states imposed by the control logic.

$$\begin{cases} V_{ab} = (1 - S_1) \cdot V_{dc1} \\ V_{bd} = (S_3 - 1) \cdot (V_{dc1} + V_{dc2}) \\ V_{df} = (1 - S_5) \cdot V_{dc2} \end{cases} \quad (4)$$

Substituting equations in equation (4) into equation (3), the converter terminal voltage at grid side can be obtained from equation (5).

$$V_{af} = V_{dc1} \cdot (S_3 - S_1) + V_{dc2} \cdot (S_3 - S_5) \quad (5)$$

Three state variables can be identified as the current through switching inductance and two capacitor voltages. The source voltage is the input variable. Defining  $x_1 = ic$ ,  $x_2 = V_{dc2}$ ,  $x_3 = V_{dc1}$ ,  $x_4 = V_{af}$  and applying the KVL on the electrical network in Figure 2, the following voltage-current relations can be written:

$$\frac{dx_1(t)}{dt} = -\frac{R}{L} x_1(t) - \frac{(S_3 - S_5)}{L} x_2(t) - \frac{(S_3 - S_1)}{L} x_3(t) + v_s(t) \quad (6)$$

$$\frac{dx_2(t)}{dt} = \frac{(S_3 - S_5)}{C} x_1(t) \quad (7)$$

$$\frac{dx_3(t)}{dt} = \frac{(S_3 - S_1)}{C} x_1(t) \quad (8)$$

The converter terminal voltage at the grid side can be written as a dependent variable in terms of switching states and state variables as follows by using equation (5).

$$x_4(t) = x_3(t) \cdot (S_3 - S_1) + x_2(t) \cdot (S_3 - S_5) \quad (9)$$

The output variable can be defined as the converter current at the grid side that is same as the current through switching inductance.

$$y = x_1(t) \quad (10)$$

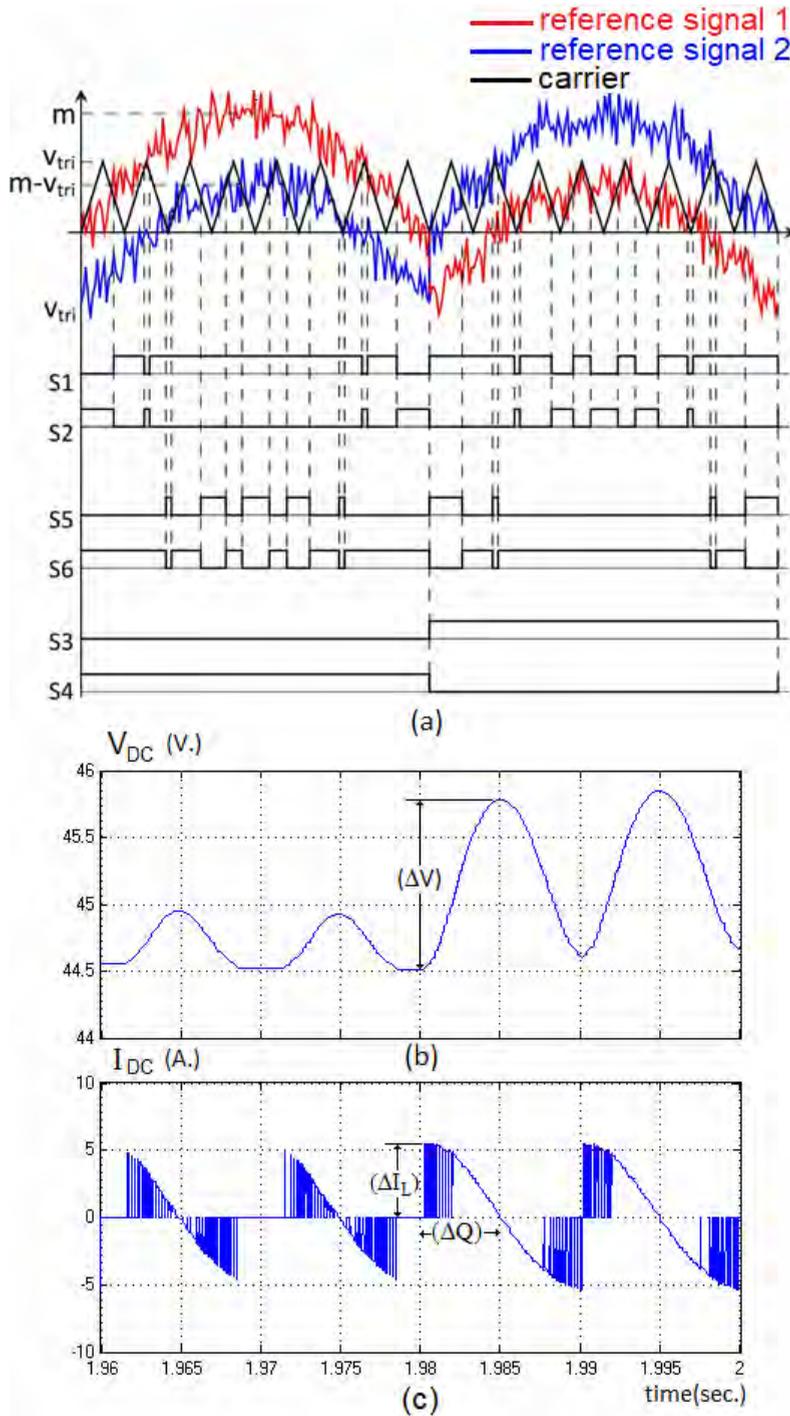
The value of the switching inductance in the converter circuit is usually selected as a function of switching frequency, ripple magnitude of line current and the level of DC link capacitor voltage (Cardenas and Molinasa, 2013).

### 3.2 Cascade controller with multilevel converter

The proposed cascade controller is used to control single-phase cross-connected U-cell converter as it is shown in Figure 2. The average value of the capacitor voltages should be the same, so their levels are measured with the help of two voltage sensors and



**Figure 4** (a) Switching logic of single-phase 5-level converter with sinusoidal reference signal over one period (b) the capacitor voltage over two periods (c) the capacitor current over two periods (see online version for colours)



The value of the DC link capacitors used in the multilevel converters plays a critical role in the compensation and performance of the system. Its value affects the harmonic content of the converter current at the source side. Figure 4(b) presents the simulation results of the capacitor voltage variation ( $\Delta V$ ) in time during two periods of source voltage (40 ms). It should be noticed that two capacitors in the multilevel converter have been swapped in each period.

The capacitors have been charged with the positive current and discharged with the negative current as it is clearly seen in Figure 4(c). The current-time area provides the change of charge in a capacitor which is formulated in equations (11) and (12). The switching ripple on the capacitor current has been neglected for estimation of the capacitor value in worst case. The integration interval relating the change of charge ( $\Delta Q$ ) to the change of capacitor current ( $\Delta I_L$ ) is depicted in Figure 4(c).

$$\Delta Q = \int_0^{\frac{\pi}{2}} I_L \cdot \cos(\omega t) dt \quad (11)$$

$$\Delta Q = \frac{\Delta I_L(\max)}{\omega} \quad (12)$$

where  $\omega = 2\pi f$  and  $f$  is at twice the supply frequency.

The value of the capacitor is estimated due to the worst case situation from equation (13).

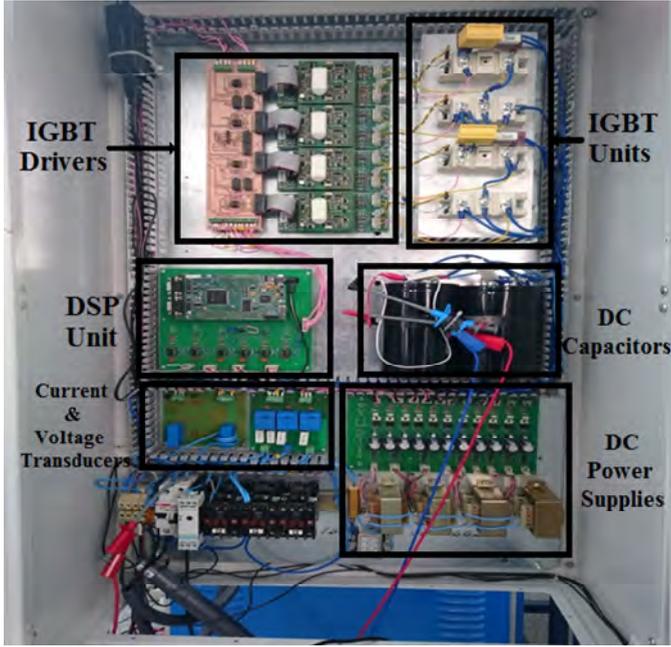
$$C = \frac{\Delta I_L(\max)}{\omega \cdot \Delta V}. \quad (13)$$

## 4 Simulation and experimental results

### 4.1 Results of simulation and experimental work

The MATLAB/Simulink is used for the simulations of two converters with the proposed controller. The supply voltage is considered as a pure sinusoidal waveform in the simulation studies and the other parameters are set to the same values of the experimental setup.

Figure 5 shows the experimental hardware designed for multi-function (H-bridge and U-cell converter up to five-level with their gate drives consisting of four half-bridge IGBTs and their gate drives) to investigate the validity of the proposed controller on SAPF and STATCOM applications. Therefore, two legs (four IGBTs) are used to realise H-bridge converter and three legs (six IGBTs) are used to realise U-cell multilevel converter in this study. The setup is reconfigured to investigate the success of controllers in Figure 1 and Figure 2 by programming the TMS320F28335 floating-point DSP board according to the application. Semikron 75GB123D IGBTs and their gate drive circuits Skyper 32Pro, voltage transducers LV25P and current transducers LA10P are used in the circuit. LeCroy 604zi oscilloscope, Fluke 438 power quality analyser and Fluke 434 energy analyser are used to measure the experimental results.

**Figure 5** Single-phase converter implemented in the laboratory (see online version for colours)

#### 4.2 H-bridge converter

The H-bridge converter is designed with the parameters given in Table 2. The load in Figure 1 has the resistive (300 W) and inductive (300 VAR) components connected in parallel to a single-phase bridge rectifier used as a nonlinear load. An inductor of  $L_0 = 25$  mH and a capacitive load ( $R_0 = 100 \Omega$  and  $C_0 = 200 \mu\text{F}$ ) are connected to the input and output of the rectifier, respectively. The capacitive and pure resistive loads are also tested, but the results are not included into the paper because of space limitation. The transfer function of the PR controller  $H_{PR}(s)$  is given in equation (14) which can be written in terms of proportional and integral gain parts. The PI parameters are  $k_i = 10$  and  $k_p = 0.5$  while the PR parameters are  $k_R = 0.01$  and  $k_p = 1$  as given in Table 2.

$$H_{PR}(s) = 2.k_p + \frac{2.k_R.s}{s^2 + \omega^2} \quad (14)$$

The results of the simulation and experimental work with nonlinear load are given in Figure 6 at steady-state operation. Source voltage and source current are shown in Figures 6(a) and 6(b), respectively. It can be seen that the source current is in phase with the source voltage. Figures 6(c) and 6(d) show the converter and load currents, respectively. The current supplied by the converter compensates the reactive power and suppresses the source current harmonics. Figure 6(e) shows the converter output voltage at the grid side behind the switching (coupling) inductance which is non-filtered PWM waveform. Figure 6(f) depicts DC bus voltage where it should be noted that spikes appeared in the experimental results are related to the noises captured by measurement instrument, as such rapid and high frequency ripples are not possible considering supply

voltage range and circuit parameters. The THD of source current, which was 12.05% before operating the converter as the SAPF and STATCOM, is reduced to 5.97% by the proposed control algorithm.

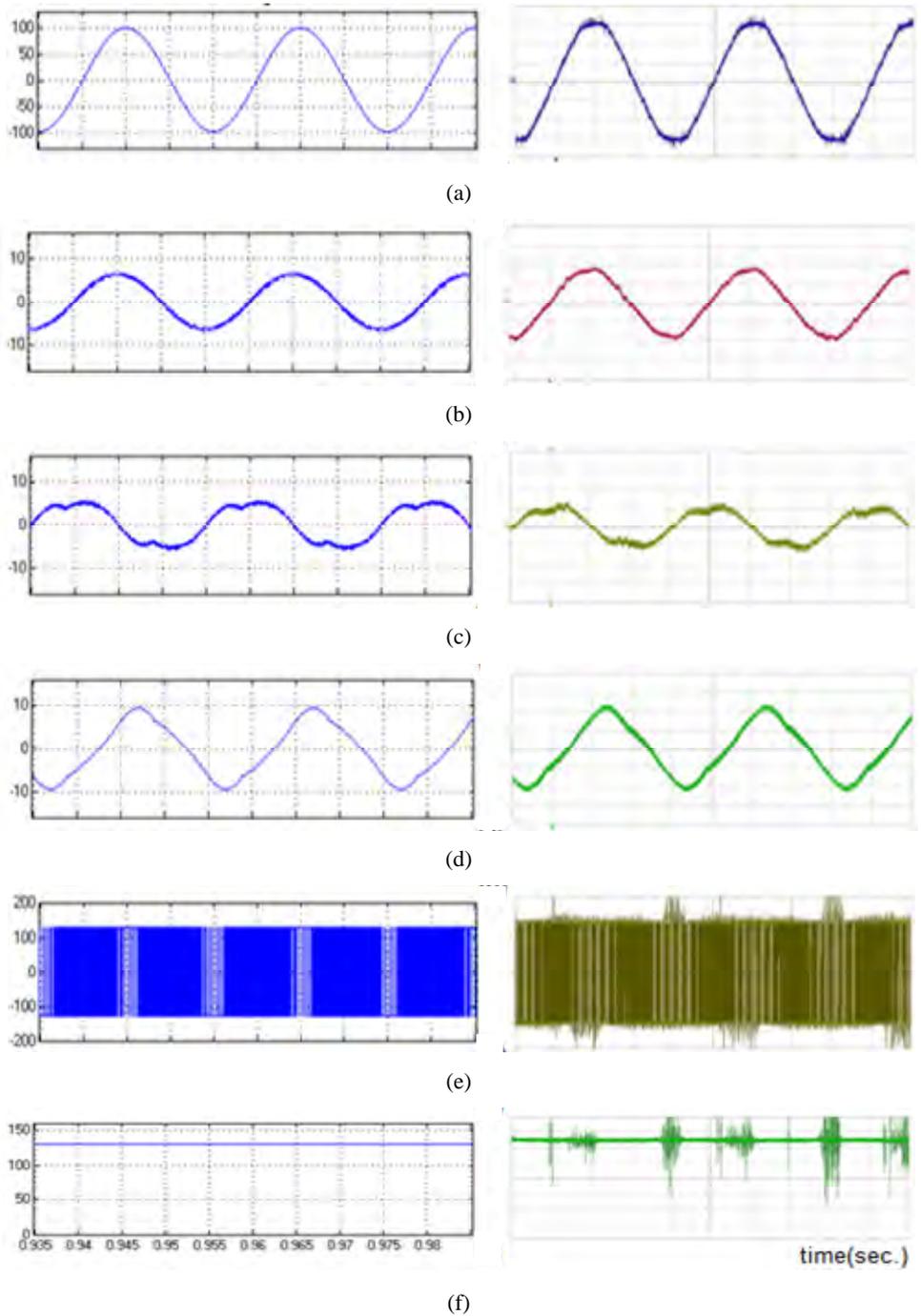
**Table 2** Parameters of simulation and experimental setup

<i>Parameters</i>	<i>H-bridge</i>	<i>Multilevel</i>
AC supply voltage	70 V (RMS)	50 V (RMS)
Fundamental frequency	50 Hz	50 Hz
DC bus reference	125 V	45 V (each)
DC bus capacitor	10,000 $\mu$ F	10,000 $\mu$ F
Load	300 W $\pm$ 300 VAR	300 W $\pm$ 300 VAR
Coupling inductance, $L$	5 mH	5 mH
Coupling resistance, $R$	0.5 $\Omega$	0.5 $\Omega$
Sampling time	50 $\mu$ s	50 $\mu$ s
Proportional gain of PI $k_p$	0.5	0.5
Integral gain of PI $k_i$	10	10
Proportional gain of PR $k_p$	1	1
Resonant gain of PR $k_R$	0.01	0.01

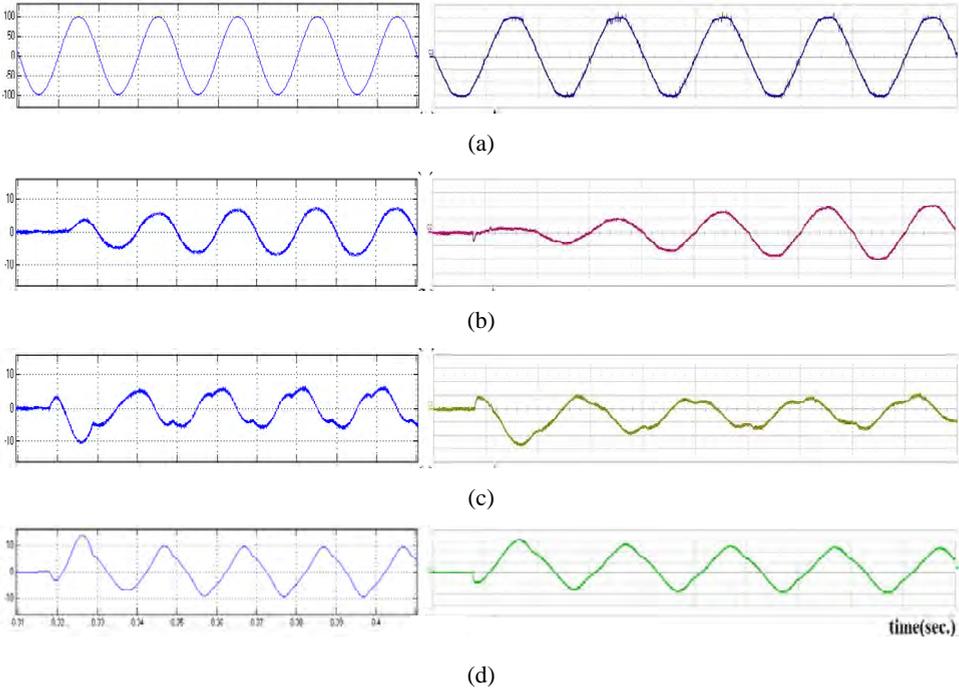
The transient response of the controller is also evaluated during the step change of load. Simulation has been carried out under no-load until  $t = 0.318$  seconds. Therefore, the DC link capacitor is charged up and the converter losses are supplied from the source during this interval. Then, the nonlinear load is switched to the grid voltage when time equals to 0.318 seconds. Figure 7 shows the results of simulation and experimental work under this loading transition. Source voltage and source current are shown in Figures 7(a) and 7(b) where Figures 7(c) and 7(d) show the converter and load currents, respectively. At  $t = 0.318$  seconds when the load is connected, load current is raised as it is shown in Figure 7(d). The converter current starts the reactive and harmonics compensations instantaneously. The source current is in phase with source voltage and the current supplied by the converter compensates the reactive power and eliminates source current harmonics.

The response of the proposed controller is also tested with the single-phase bridge rectifier drawing highly distorted supply current. The rectifier input in Figure 1 is fed by the source voltage through an inductor of  $L_0 = 5$  mH and the output terminal is connected to a lower value of resistance in parallel to the capacitor ( $R_0 = 20 \Omega$  and  $C_0 = 200 \mu$ F). While the converter is operating at no-load and keeping the regulated DC capacitor voltage around the reference level, the load is switched to the power supply at  $t = 0.3$  seconds. The supply voltage, supply current, converter current and load current variations in time during the transient and steady-state operation are given in Figures 8(a)–8(d), respectively. The load (single-phase diode bridge rectifier) current in Figure 8(d) has high THD equal to 64.27%. The H-bridge converter working as SAPF and STATCOM with proposed controller has effectively estimated and compensated harmonic current of the load as it is shown in Figure 8(c). Therefore, the supply current THD is reduced to 6.37% which is within standard limits.

**Figure 6** Simulation (left) and experimental (right) results of R-L and nonlinear load at steady-state for H-bridge, (a) supply voltage (33 V/div) (b) supply current (4 A/div) (c) converter current (4 A/div) (d) load current (4 A/div) (e) converter voltage (100 V/div) (f) DC bus capacitor voltage (50 V/div), time (5 ms/div) (see online version for colours)



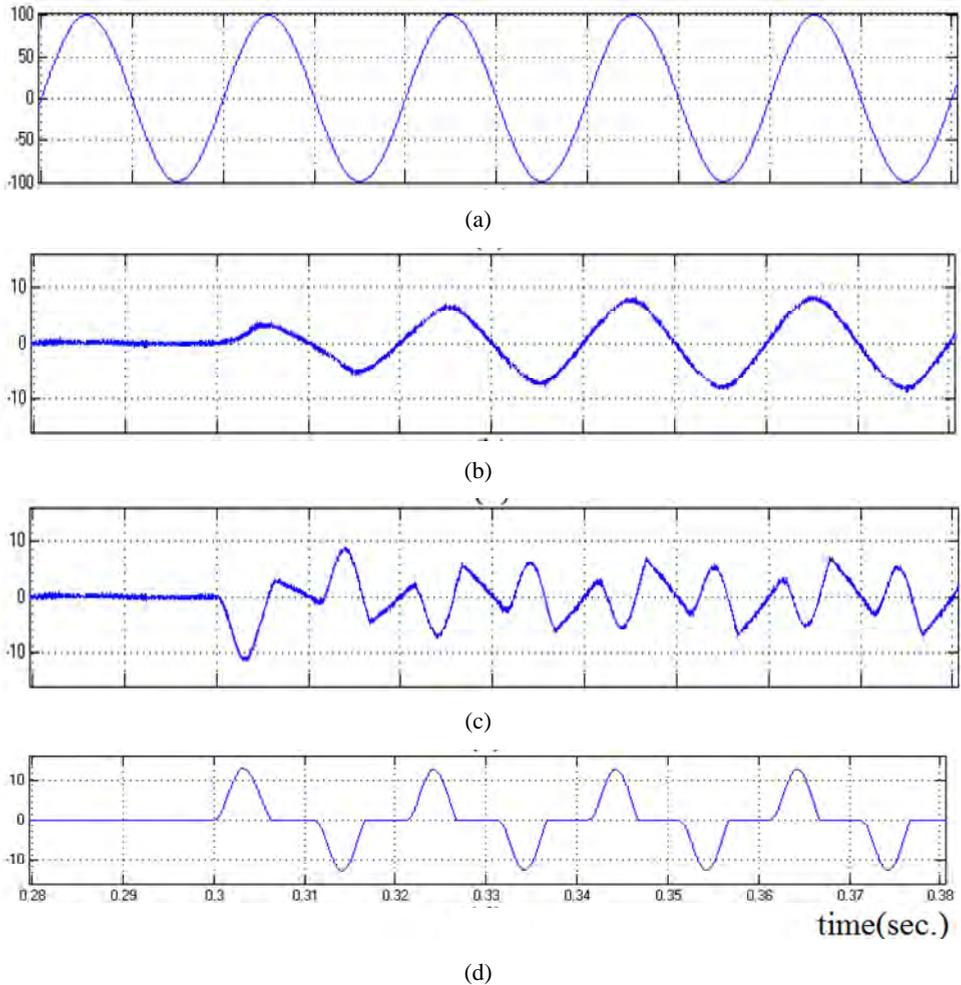
**Figure 7** Simulation (left) and experimental (right) results for starting R-L with nonlinear load for H-bridge, (a) supply voltage (33 V/div) (b) supply current (4 A/div) (c) converter current (4 A/div) (d) load current (4 A/div), time (10 ms/div) (see online version for colours)



### 4.3 Multilevel converter

The simulation and experimental results of the controller with the cross-connected U-cell multilevel converter have been presented in this section to illustrate the performance of controller on nonlinear loads. The single-phase converter has been tested under inductive nonlinear load. The supply voltage is set to 50 volts RMS via a single-phase autotransformer and each DC capacitor voltage's reference value is set to 45 volts DC. The five-level U-cell converter has a 5 mH switching (coupling) inductor and two 10,000  $\mu\text{F}$  DC link capacitors with 22 k $\Omega$  discharge resistors. The load has the resistive (200 W) and inductive (100 VAR) components connected in parallel to a single-phase bridge rectifier. In nonlinear load, an inductor of  $L_0 = 25$  mH and the resistive-capacitive load ( $R_0 = 100 \Omega$  and  $C_0 = 200 \mu\text{F}$ ) are connected to the input and output of the rectifier, respectively as it is shown in Figure 2. For PI controllers and PR controller gains, given in Table 2, the same settings as per for H-bridge converter are used.

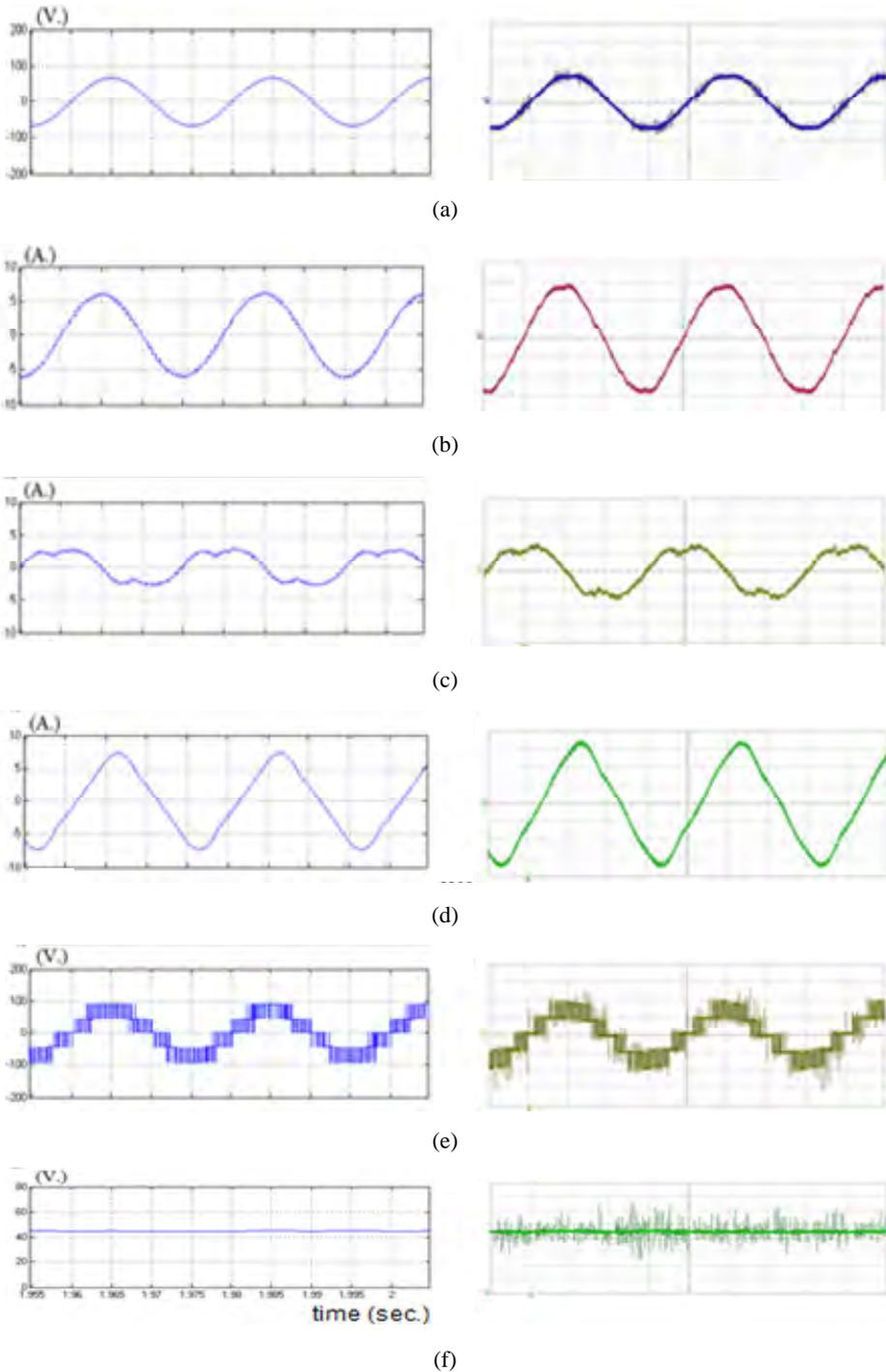
**Figure 8** Simulation results of nonlinear load at transient for H-bridge converter; (a) supply voltage (b) supply current (c) converter current (d) load current (see online version for colours)



The simulation and experimental results at steady-state condition are illustrated in Figure 9. The supply voltage and supply current are in phase as shown in Figures 9(a) and 9(b), respectively while the non-sinusoidal load current is shown in Figure 9(d). The converter current is non-sinusoidal capacitive current as shown in Figure 9(c). The converter works as the SAPF and STATCOM compensating the reactive power and current harmonics of the load. The THD of compensated source current is measured to be 3.7% in Figure 9(b).

The converter voltage is shown in Figure 9(e) and the RMS value of its fundamental component is slightly greater than the supply voltage to supply the reactive towards the load. The logic of PWM operation for five-level output voltage is clearly observed on the waveform in Figure 4. The average value of the DC capacitor voltage is retained at the reference value with the help of the swapping algorithm and PI controllers as shown in Figure 9(f).

**Figure 9** Simulation (left) and experimental (right) results of R-L load, (a) supply voltage (50 V/div) (b) supply current (2 A/div) (c) converter current (2 A/div) (d) load current (2 A/div) (e) converter voltage (50 V/div) (f) DC bus capacitor voltage (10 V/div), time (5 ms/div) (see online version for colours)



Comparing the results of the H-bridge converter and U-cell multilevel converter, it can be noticed that SAPF and STATCOM with U-cell structure has superior performance and it can achieve lower THD level with lower voltage level at DC bus. It should be mentioned that one should assess the increased number of component (and initial cost of the device) evaluating this superior performance. More detail on comparison of these two topologies is beyond scope of this paper as the main purpose of this paper is to evaluate the effectiveness of the proposed control method with two converter structures and validate the results by experimental setup.

## 5 Conclusions

The PR controller is used in cascade structure with the PI in order to control the source current and DC capacitor voltage during the reactive power compensation and harmonic current elimination. The actual current tracks the reference sinusoidal current with a novel approach on resonant controllers based on error minimisation. Since the controller is operated at power frequency of 50–60 Hz, the time delay of digital processor is not significant for controller operation, hence it is not taken into consideration. All the controllers and the single-phase PLL have been programmed on the floating-point DSP. The simulation results are verified on the single-phase H-bridge and U-cell converters for reactive power compensation and harmonic current elimination. Successful implementation of proposed cascade controller showed meritorious performance compensating reactive power and harmonic current both in transient and steady-state conditions.

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