Carrier depletion type PIN phase shifter in silicon MZM for 200 Gbps operation

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Abstract: Silicon-based photonic modulators are a primary choice for on-chip optical devices with CMOS fabrication compatibility. The phase shifter in a silicon photonics modulator plays a significant role in determining the efficiency of the modulator to meet the optical data communication’s future demands. Obtaining high extinction ratio (ER) and with acceptable bit error rate (BER) at low voltage and low loss was kept as the primary objective for the proposed PIN phase shifter in an unbalanced silicon Mach-Zehnder modulator. The phase shifter length was kept at 2 mm, and the carrier doping region was reduced to decrease the carrier absorption loss. The concentration of P and N in the phase shifter was set to $7 \times 10^{17}$ cm$^{-3}$ and $5 \times 10^{17}$ cm$^{-3}$, and the
intrinsic gap was varied (50, 100, 150, 200, 250, 300, 350 and 450 nm) for the study to obtain the optimum gap to meet the objective. For 200 Gbps, the proposed modulator with intrinsic gap 150 nm obtained 18.68 dB ER having $\text{VrL} = 0.8 \text{ V.cm}$. Insertion loss obtained for the phase shifter was 3.421 dB/cm. The proposed design is expected to enhance the performance of silicon optical modulators for commercial applications, and also other applications such as optical switches, delay lines, and optical interconnect.

**Keywords:** SiPh; silicon photonics; PIN phase shifter; MZM; Mach-Zehnder modulator; ER; extinction ratio; BER; bit error rate.


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1 Introduction

Carrier depletion type phase shifter is used to realise high speed and energy-efficient silicon modulators [1]. Mach-Zehnder interferometer (MZI) modulators are preferred as they can guarantee broadband/high-speed operation, large thermal tolerance and can be fabricated by using a cost-effective CMOS compatible process [2,3]. The modulation efficiency of a phase shifter is determined by the change in concentration of carrier with respect to the applied voltage and thus capacitance. Capacitance is inversely proportional to power consumption, as an increase in carriers needs low voltage to provide the concentration variation needed for phase shift [4]. Higher capacitance leads to low $V_{\pi L}$, i.e., the voltage $V_{\pi}$ required to obtain a $\pi$ phase shift along with the phase shifter of length $L$ [5]. The depletion width has to be reduced, and carrier concentration has to be increased, in order to increase the capacitance and thus the modulation efficiency. The disadvantage is, it increases the carrier absorption loss. Thus this leads to the trade-off to obtain high capacitance and low loss [4]. Various phase shifter design patterns have been proposed to obtain high modulation efficiency. The dopants are reduced where it leads to high absorption loss and increased at places that leads to high capacitance [5]. Doping concentration, doping pattern and intrinsic gap play a significant role in determining the performance of a phase shifter [3–18]. The primary two types are the vertical and lateral PN junction. Though vertical PN junction provides higher modulation efficiency when compared to the traditional method, it is not preferred due to fabrication difficulties [6]. The interleaved PIN junction increases the capacitance at the cost of power consumption and reduced bandwidth and has design challenges [7,9]. De Farias et al. [18] demonstrated that silicon modulators could perform for high-speed operations.
The lateral PIN type carrier depletion based phase shifter is preferred as it easy to fabricate, lower absorption loss, low cost and suitable for high-speed applications. In the study, intrinsic gaps were varied in order to find the optimum gap for better modulation efficiency. The proposed design is explained in Section 2. The results and the corresponding analysis are discussed in Section 3, and the paper concludes in Section 4.

2 Design structure

Traditional PIN phase shifters are based on the large thickness of the doped region, which results in higher absorption losses. This may be circumvented by reducing the doping area. One such idea is to confine the doping in the slab region. Figure 1 shows the light propagation (TE<sub>1</sub> mode) through the waveguide along the y-axis. The x-axis and z-axis denote the width and thickness of the waveguide. The y-axis denotes the length of the waveguide. The thickness of the waveguide is set to 220 nm as per fabrication standards and the width of the waveguide set to 500 nm to support TE<sub>1</sub> mode for modulation. The doping was concentrated in the slab region so that to reduce the dopant exposure area to the light confined path. The concentration of P and N in the phase shifter is set to $7 \times 10^{17}$ cm<sup>-3</sup> and $5 \times 10^{17}$ cm<sup>-3</sup> such that the concentration of holes higher than electrons to have a higher index shift with minimum absorption [10]. The doping concentrations of both P++ & N++ is $1 \times 10^{19}$ cm<sup>-3</sup> to reduce access resistance. Aluminium electrodes are preferred for better electrical contacts, and driving voltage was set to 0–5 V to keep the voltage consumption minimal.

Figure 1 Light transmission (see online version for colours)

Figure 2 shows that only the slab region is used for doping, and the intrinsic region is further used to reduce the carrier absorption loss. The phase shifter length (PS) is set to 2 mm, and the intrinsic gap ($W_i$) is varied ($W_i = 50$, 100, 150, 200, 250, 300, 350 and 450 nm), the corresponding results are obtained and tabulated for analysis.
3 Results and discussion

The simulation process (Figure 3) comprises two parts (a) device-level simulation and (b) system-level simulation. Commercially available Lumerical tool (Version: S2019A-R1) was used for the simulation analysis. In the device level simulation (Figure 3(a)) the electro-optic characteristics of the phase shifter were analysed using the Finite-Difference Eigenmode (FDE) analysis. Lumerical Mode and Lumerical Device (Charge Transport) module were used for device-level simulation. The obtained phase shifter’s parameter values were imported into an MZM in Lumerical Interconnect module, and the system-level simulation (Figure 3(b)) was performed.

The RC equivalent electrical circuit of the PIN structure is shown in Figure 4. The PIN junction acts as a capacitor in reverse bias with P and N regions acting as the side plates and the intrinsic region as a dielectric of the capacitor. The slabs on the P and N doped regions along the slabs form the resistive region. The capacitance decreases while the intrinsic gap widens.

The proposed phase shifter design is optimised by varying the \( W_i \). Figure 5 shows the capacitance variation with the change in voltage for different \( W_i \) in the proposed phase shifter of length 2 mm. The carrier concentration for P and N doped region set to \( 7 \times 10^{17} \) cm\(^{-3} \) and \( 5 \times 10^{17} \) cm\(^{-3} \), respectively. The capacitance per unit length varies with the change in the carrier concentration with respect to the increase in voltage \( V \) and \( W_i \). It is noted that as the \( W_i \) increases the carrier concentration reduces, and therefore the capacitance reduces with \( W_i \). The movement of charge carriers depleted in reverse bias causes the capacitance to further reduce with the application of \( V \). This change in carrier concentration leads to the variation in the effective index \( (\Delta n_{\text{eff}}(V)) \) (1) of the phase shifter (Figure 6) which in turn causes the phase shift \( \phi \) (2) in the light (Figure 7).

\[
\Delta n_{\text{eff}}(V) = n_{\text{eff}}(V) - n_{\text{eff}}(0) \\
\phi = \frac{2\pi \Delta n_{\text{eff}}(V)L}{\lambda} 
\]
Figure 3  Simulation process flow chart: (a) device-level simulation and (b) system-level simulation

(a) Device Level Simulation
Lumerical Mode → Lumerical Device (CT) → Lumerical Mode

- Designing rib Waveguide
- Proposed Phase shifter design
- Calculating Cup vs. Voltage
- FDE Analysis
- Calculating the change in Effective Index, Phase shift and Loss with respect to Voltage

(b) System level Simulation
System level Simulation → Lumerical Interconnect

PRBS Generator → Electrical Signal Generator → Eye Diagram Analyser
Laser → Modulator → Photo detector

Figure 4  The simplified equivalent electrical circuit diagram for PIN structure

\[ \frac{1}{C} \]

Figure 5  Capacitance variation with \( V \) for various \( W_i \) (see online version for colours)
The widening of the intrinsic region reduces the carrier concentration, which is responsible for the effective index variation and thereby reduces the phase shift. The decrease in carriers causes the carrier absorption loss to reduce, thus decreasing the loss with increase in $W_i$ (Figure 8). The carriers get depleted with the application of voltage which further reduces the loss. The proposed phase shifter is tested in an unbalanced MZM with the length variation of 100 µm between the waveguide arms. The transmission per wavelength for $T(V)$ is calculated using equation (3),

$$
T(V) = \left| \frac{1}{1 + \frac{\sigma \exp \left( \frac{2\pi\Delta n_{\text{eff}}(V)L}{\lambda_0} \right)}{\exp(-\varphi)}} \right|^2
$$

(3)
Figure 8  Loss vs. $V$ for $W_i$ (see online version for colours)

The transmission spectra lie between $\lambda = 1553.4$ nm to 1553.7 nm, and the wavelength 1553.5 nm is selected for detailed study. In order to study the $W_i$ variations in the modelled PIN structure, system-level simulation analysis was performed at 20 Gbps with NRZ coding technique for pseudo-random bit sequence (PRBS). At 4 V and $W_i = 150$ nm, an ER of 19.25 dB and BER of $4.59 \times 10^{-15}$ was obtained. The eye diagram obtained (Figure 9) has wider eye-opening, a rise time ($t_r$) of 5 ps, the fall time ($t_f$) of 9.4 ps and lower jitter, which ensures high-speed data transmission applications. It is observed that the eye-crossing is at 26%, which denotes that the timing for zero pulses is higher than one pulse in the data transmitted [19,20]. The time distortions for the pulses are calculated by duty cycle distortion (DCD) (4),

$$\text{DCD} = \frac{100 \times (\text{time difference between rise and fall edges at 50\% level})}{\text{Bit period}}$$

When the DCD value deviates from 0\%, it leads to the error at reception, causing BER to increase. DCD is calculated to be 5.13\% due to steep rise and fall time along with open eye.

In Table 1, ER and BER values are tabulated for higher bit rates to study the feasibility of the device. At the higher bit rate, the pulses corresponding to ‘1’ state get into an error which causes the BER to increase and due to this ER reduces. The energy per bit is calculated to be 1.72 pl/bit, and the bandwidth of the modulator is 28 GHz. It is found that the proposed phase shifter works for 200 Gbps with 18.6 dB ER and $4.57 \times 10^{-04}$ BER, which is below the standard forward error correction (FEC) threshold of $3.8 \times 10^{-03}$. The parameters obtained for the proposed PIN phase shifter is compared with other published results in Table 2. Trade-off conditions between the parameters play a vital role in designing a phase shifter. In Félix Rosa et al. [13], the length of the phase shifter was reduced to 0.5 mm but at the expense of loss (7 dB/cm). Higher ER (>25 dB) was obtained in Zhou et al. [15] at the cost of high VπLπ of 4.1 V.cm. In Rao et al. [16], an ER of 18 dB was obtained, but a phase shifter length of 8 mm was required.
Interleaved PN junction with reduced length designed by Jeeva and Boddu [19] was used in 50 Gbps data transmission with $V_{πL}$ of 2.4 V.cm. The proposed phase shifter was designed with consideration of the trade-off conditions. The intrinsic gap ($W_i = 150$ nm) and rib region (un-doped) reduced the losses, but at the same time produced high ER with acceptable BER at low $V_{πL}$ of 0.8 V.cm.

**Figure 9**  Eye diagram for 2 mm PS with $W_i = 150$ nm at 4 V (20 Gbps) (see online version for colours)

<table>
<thead>
<tr>
<th>Gbps</th>
<th>$ER$ (dB)</th>
<th>$BER$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>19.25</td>
<td>$4.59 \times 10^{-15}$</td>
</tr>
<tr>
<td>80</td>
<td>18.98</td>
<td>$3.59 \times 10^{-06}$</td>
</tr>
<tr>
<td>200</td>
<td>18.68</td>
<td>$4.57 \times 10^{-04}$</td>
</tr>
</tbody>
</table>

**Table 1**  ER and BER for varying Gbps for 2 mm PS with $W_i = 150$ nm at 4 V

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$λ$ (nm)</th>
<th>Length (mm)</th>
<th>Gbps</th>
<th>$V_{πL}$ (V.cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[11]</td>
<td>~1558</td>
<td>0.75</td>
<td>60</td>
<td>1.6</td>
</tr>
<tr>
<td>[12]</td>
<td>1541</td>
<td>2.5</td>
<td>25</td>
<td>2</td>
</tr>
<tr>
<td>[13]</td>
<td>1550</td>
<td>0.5</td>
<td>–</td>
<td>3.1</td>
</tr>
<tr>
<td>[14]</td>
<td>~1545</td>
<td>1.5</td>
<td>50</td>
<td>2.4</td>
</tr>
<tr>
<td>[15]</td>
<td>~1571</td>
<td>3.9</td>
<td>–</td>
<td>4.1</td>
</tr>
<tr>
<td>[16]</td>
<td>1550</td>
<td>8</td>
<td>–</td>
<td>3.1–6.5</td>
</tr>
<tr>
<td>[17]</td>
<td>~1550</td>
<td>5</td>
<td>100</td>
<td>2.5</td>
</tr>
<tr>
<td>[18]</td>
<td>1551</td>
<td>1.5</td>
<td>112</td>
<td>2.3</td>
</tr>
<tr>
<td>This work</td>
<td>1553.5</td>
<td>2</td>
<td>200</td>
<td>0.8</td>
</tr>
</tbody>
</table>
4 Conclusion

Carrier depletion type silicon PIN phase shifter was proposed and analysed in this paper. The intrinsic gap of the proposed phase shifter of length 2 mm was varied ($W_i = 50, 100, 150, 200, 250, 300, 350$ and 450 nm) and analysed. An optimum intrinsic gap of $W_i = 150$ nm was found to obtain 18.68 dB ER for 200 Gbps, having $V_{\pi L} = 0.8$ V.cm. The eye diagram obtained ensures that the designed phase shifter is suitable for inter and intra data centre applications. It also finds other applications like delay lines, optical switches, optical fibre communication, free space optics etc. In future, dense wavelength division multiplexing technique of multiplexing multiple wavelengths with a mixed bit rate and modulation formats can be implemented.

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