A comparative analysis of the short-channel effects of double-gate, tri-gate and gate-all-around MOSFETs

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Abstract: The electrical characteristics of metal-oxide semiconductor field-effect transistors (MOSFETs) deteriorate with the scaling of device dimensions. To further the miniaturisation and to have more control over the channel, one of the promising solutions is the multi-gate (MG) architecture of MOSFET. In the present work we have investigated various MG devices like double-gate (DG), tri-gate (TG) and gate-all-around (GAA) MOSFETs by varying their physical parameters and have compared the associated short-channel effects (SCEs). For a specific SCE, a common mathematical expression has been used for all the MOSFET architectures. The analytical results have been found to be in reasonable agreement with the simulated/ fabricated devices.

Keywords: multi-gate; MG; double-gate; DG; tri-gate; TG; gate-all-around; GAA; MOSFET; short-channel effects; SCEs; quantum mechanical effect.

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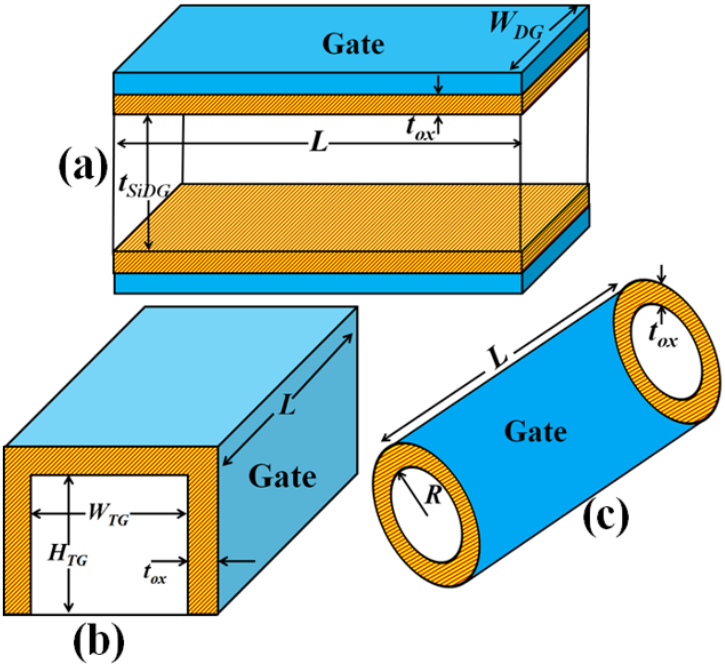
1 Introduction

The ever shrinking dimensions of metal-oxide semiconductor field-effect transistors (MOSFETs) have resulted in unexpected electrical characteristics of the devices, such as lowering of threshold voltage due to increase in drain terminal voltage and decrease in the channel length. Various techniques have been proposed in the literature to alleviate such short-channel effects (SCEs) (Oh et al., 2000; Baral et al., 2016; Tiwari et al., 2012; Kumar and Kumari, 2017). The main objective of all these studies is to explore the methods by which the flow of charge in the MOSFET channel is suitably controlled by the gate. In multi-gate (MG) architecture, e.g., as shown in Figure 1, the gate terminals contribute more electric field to the channel region than the source (S)/drain (D) terminals and therefore MG devices have more control over channel region (Ferain et al., 2011). Therefore several MG MOSFETs have been analysed so far (Colinge, 2004; Chanda et al., 2015; Kumar and Jha, 2013; Fossum et al., 2003; Saha et al., 2015).

A number of analytical models pertaining to the SCEs of MG MOSFETs are available in the literature and are based on how the associated differential equations have been solved (Yu et al., 2007; Xie et al., 2010; Kumar and Mahapatra, 2010) with each having its own merits and limitations (Xie et al., 2012). Several studies have been done to analyse the effect of variation of device dimensions on the SCE of MG devices but most of them examined either a double-gate (DG) (Chen et al., 2003), or tri-gate (TG) (Dhanaselvam and Balamurugan, 2013) or gate-all-around (GAA) (El Hamid et al., 2007) MOSFET. There are also some analysis reports comparing more than one architecture, but they are mostly simulated ones (Park and Colinge, 2002; Poiroux et al., 2005). Finding the analytical solution of Poisson's equation becomes difficult when depletion charges and other nonlinear effects are taken into consideration. Furthermore, for a simulator to save on computational time it is better to have a common differential equation to solve than multiple equations related to different gate architectures. By additionally incorporating geometrical transformations in the solution of DG devices, the physical effects of other MG devices can be accurately ascertained (Duarte et al., 2013).

In Jha and Choudhary (2018), the impact device parameters on the threshold voltage of DG, TG and GAA MOSFETs were investigated. All those analysis were done for a constant drain voltage. For short channel devices, the channel length gets modulated by the applied drain voltage and therefore threshold voltage could not remain constant with the change in drain terminal voltage. Therefore it becomes necessary to include the contribution of drain voltage in the calculation of threshold voltage. In this present work we have incorporated the effect of drain voltage in all the calculations which ultimately improves the electrical representation of the device characteristics. The additional work that we have carried out in this paper is the investigation of SCEs, such as drain-induced barrier lowering (DIBL) and subthreshold swing (SS) for DG, TG and GAA MOSFETs. The distinctiveness of the present work is that it extends the analytical expressions related to SCEs of DG MOSFETs to TG and GAA MOSFETs without any adjusting parameters. Channel length and thickness have been varied to observe the changes in SCEs for various MG devices.

Figure 1 Structure of MG architectures, (a) DG (b) TG (c) GAA MOSFETs (see online version for colours)



2 Theoretical details

The Poisson equation can be written as $\partial^2\psi / \partial x^2 + \partial^2\psi / \partial y^2 = q\,(n + N_A) / \varepsilon_o\varepsilon_{Si}$ where ψ is the potential in the channel and n is the inversion charge density and N_A is the p-type doping concentration. This equation can be solved by using an appropriate potential expression (Chen et al., 2003) in the channel and through proper boundary conditions. The threshold voltage is defined as the value of V_{gs} at which the inversion charge density reaches its threshold value (Q_{th}) suitable for turning the device ON (Hamdy et al., 2006; Ray and Mahapatra, 2009). Dependency of the threshold voltage on the drain terminal voltage has been accounted for by the term ηV_{ds}, where η is the DIBL and given as (Tsormpatzoglou et al., 2008) $\eta = B\,[V_{bi} - V_{th}\,ln\,(Q_{th} / n_i t_{Si})]^{0.5}\,\{[V_{bi} + V_{d,high} - V_{th}\,ln\,(Q_{th} / n_i t_{Si})]^{0.5} - [V_{bi} + V_{d,low} - V_{th}\,ln\,(Q_{th} / n_i t_{Si})]^{0.5}\} + C\,(V_{d,high} - V_{d,low})$, where $B = 2e^{L/2\lambda}\,(1 + e^{L/\lambda}) / (e^{L/\lambda} - 1)^2$, $C = (2e^{3L/\lambda} - 4e^{2L/\lambda} + 2e^{L/\lambda}) / (e^{L/\lambda} - 1)^4$, λ is the natural length and other symbols have their usual meanings. The resultant threshold voltage is expressed as $V_{th} = V_{th0} - \eta V_{ds}$. The SS is modelled by the expression (Chen et al., 2002) $SS = [1 - 2\Gamma_1\,(V_1 + V_{DS} / 2) / (V_1\,(V_1 + V_{DS}))^{0.5}\cos(d_{eff}/\lambda_1)\,e^{-(L/2\lambda 1)}]^{-1}.\,(kT/q)\,ln\,(10)$ where the symbols are as given in Chen et al. (2002). A similar incorporation of DIBL in the threshold voltage expression and subthreshold slope degradation has been reported in Smaani et al. (2013).

The DIBL and SS models of DG MOSFETs have been leveraged to analyse the behaviour of other MG devices through equivalent device parameters. The corresponding

equivalent physical dimensions of TG MOSFETs with respect to DG MOSFETs are expressed as (Duarte et al., 2013):

$$t_{SiDG} = \frac{1}{\left[\frac{W_{TG}}{2H_{TG}(2H_{TG}+W_{TG})} + \frac{2H_{TG}}{W_{TG}(2H_{TG}+W_{TG})}\right]}$$

$$t_{oxDG} = (2H_{TG}+W_{TG})\left[\frac{4.53}{\ln\left(1+\frac{3t_{ox}}{2H_{TG}}\right)} - \frac{1.25}{\ln\left(1+\frac{5t_{ox}}{4H_{TG}}\right)} + \frac{1.25}{\ln\left(1+\frac{5t_{ox}}{W_{TG}}\right)}\right]$$

$$W_{DG} = H_{TG} + 0.5\,W_{TG}$$

where t_{SiDG} and t_{oxDG} are the silicon and oxide thickness respectively of DG MOSFETs; H_{TG}, and W_{TG} are related to TG MOSFETs as given in Figure 1. Similarly, for GAA MOSFETs the corresponding dimensions of DG MOSFETs are $t_{SiDG} = 2R$, $t_{oxDG} = R \ln (1 + t_{ox} / R)$ and $W_{DG} = \pi R$.

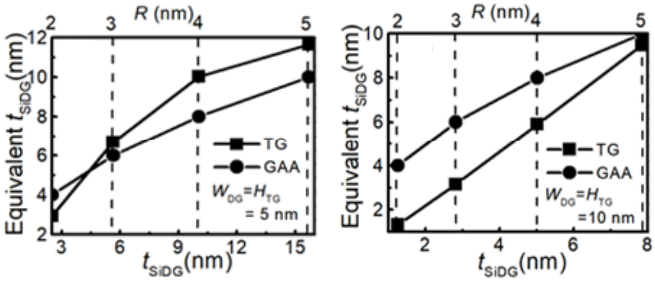
One of the ways to reduce SCEs in MOSFETs is to shrink its channel thickness. But this results in increase in transverse electric field of the inversion layer. Due to the strong field, energy band near the surface splits into quanta of energy sub-bands. The quantisation of continuous energy band increases the gate voltage required for moving the charge carriers from valence band to conduction band. This quantisation phenomenon is known as quantum mechanical (QM) effect and it leads to the increase in the threshold voltage of the device and is expressed as $\Delta V_{thQM} = (h^2 / 4qm^* t_{Si}^2)(\Delta t_{Si} / t_{Si})$ (Wong et al., 1998), where h is the Plank constant and m^* is the electron effective mass. $\Delta t_{Si}/t_{Si}$ is the magnitude of the process tolerance of t_{Si}. During fabrication processes there are chances that the device shape/dimensions may deviate from its intended form thereby affecting the threshold voltage (Li et al., 2005; Ng et al., 2009; Sharma and Kumar, 2017; Jha et al., 2014). Effective mass depends on the orientation of the Si crystal and different values can be chosen to describe devices more accurately (Colinge et al., 2006). In this work, a constant effective mass of 0.19 m_0 corresponding to Δ1-valleys of [110] orientation of Si is taken which is valid from subthreshold to saturation regions of MOSFET operation and takes into account transverse confinement (Bescond et al., 2005). There are various reported techniques through which Poisson and Schrödinger equations have been solved consistently to mathematically model the QM effect (Wong et al., 1998; Gnani et al., 2004; Roldan et al., 2008, 2010). An observation which is common in these literatures is that the increase in threshold voltage due to the quantisation of energy band is inversely proportional to the cross-section area (CSA) of the channel. Furthermore, empirical expression relating the channel thickness to the change in threshold voltage arising due to QM effect also indicates the inverse association with CSA (Roldan et al., 2008). Taking all these observations into consideration, using CSA we have extended the quantum threshold modelling of DG MOSFET to study the change in threshold voltage of TG and GAA MOSFETs. We have used the effective CSA (Jha and Choudhary, 2018) to apply the ΔV_{thQM} of DG to TG and GAA MOSFETs. To validate our analysis, we compared the *DIBL* (~39 mV/V) and *SS* (~76 mV/decade) values of the fabricated GAA MOSFET [L = 25 nm, d_{eff} = 8.03 nm (Nayak et al., 2014), t_{ox} = 1.5 nm] (Bangsaruntip et al., 2009) with our results for the same dimensions. The DIBL and SS were found to be

40 mV/V and 76.8 mV/decade respectively which are in agreement with the values reported for fabricated devices.

3 Results and discussion

For our computations we have considered undoped channel with length L and gate-oxide thickness t_{ox} to be 25 nm and 1.5 nm respectively, otherwise stated. Metal gate with mid-gap work function and S/D doping of 10^{20} cm^{-3} have been used. The SCE depends on the physical dimensions of the device. The equivalent Si thickness variation for MG architectures is shown in Figure 2. It can be seen that the choice of channel width dictates the equivalent thicknesses of DG MOSFET.

Figure 2 Variation of equivalent silicon thickness of MG MOSFETs for $W_{DG} = H_{TG}$, (a) 5 nm (b) 10 nm



(a) (b)

The effect of channel length on the reduction of the threshold voltage of different MG devices is shown in Figure 3. While reducing the channel length, when it becomes comparable to the source and drain depletion widths, the effective number of charge carriers required for device turn-on decreases, therefore there is lowering of threshold voltage. This lowering is more pronounced in DG and TG than GAA MOSFET. This in turn is due to the presence of electric field from all sides in GAA architecture.

Figure 3 Threshold voltage roll-off of MG MOSFETs having equal area of cross sections and t_{ox} = 1.5 nm

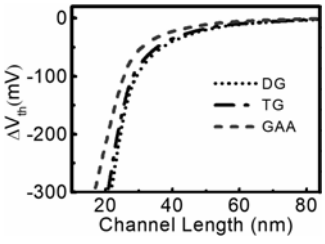
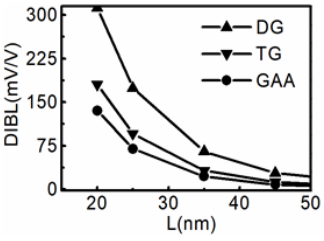


Figure 4 shows the variation of DIBL as a function of channel length for MG architectures. As channel length is reduced and drain voltage is increased, the drain depletion width increases towards the source giving rise to strong electric field from drain to source. This decreases the potential barrier at the source and as a consequence, more

number of charge carriers are able to move from source to drain through the channel. The resulting drain induced barrier lowering is more evident in DG than other MG devices. In GAA device the gate electric field is more dominant than S/D fields and therefore shows the least DIBL among all structures.

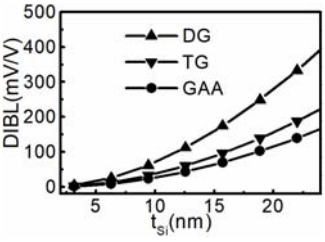
Figure 4 Variation of DIBL with the channel length for different MG MOSFETs



Note: Area of cross section of all devices are taken to be equal and t_{ox} = 1.5 nm.

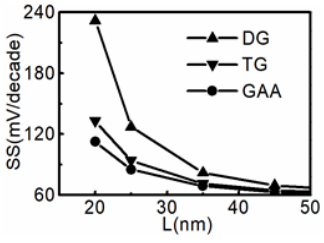
Figure 5 shows the variation of DIBL with respect to silicon channel thickness. When t_{Si} increases, the strength of gate electric field in the channel decreases (in conventional bulk MOSFET it is negligible in the substrate) but the electric field due to S/D depletion regions remains same (due to fixed L). Because of this the S/D field dominate in the channel thereby lowering the energy barrier for charge carriers and hence DIBL increases with increase in the channel thickness. To obtain the required tolerance in the variation of the threshold voltage due to DIBL, smaller channel thickness is preferred as it shows less drain induced barrier lowering. But the choice of channel thickness is constrained by the quantum effects which come to picture when channel thickness is in the nanometre regime as discussed in the theoretical section above.

Figure 5 Variation of DIBL with the channel thickness for different MG MOSFETs



Note: Area of cross section of all devices are taken to be equal and t_{ox} = 1.5 nm.

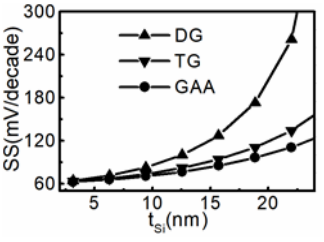
Figure 6 Variation of SS with the channel length for different MG MOSFETs



Note: Area of cross section of all devices are taken to be equal and t_{ox} = 1.5 nm.

One of the important requirements in subthreshold region of MOSFET operation is that device should turn off as soon as gate voltage reduces below threshold voltage. This characteristics is measured through the *SS* which should be as small as possible. The variation of SS as a function of channel length and thickness are depicted in Figures 6 and 7 respectively. For short channel devices, SS is more and it further increases as the channel thickness is increased. Among all MG devices, again the GAA architecture shows the least SCE in terms of SS. Digital circuits are very much sensitive to the turn on/off characteristics of the device and therefore a trade-off exists between the electrical integrity of the circuit and the packing density of the chip.

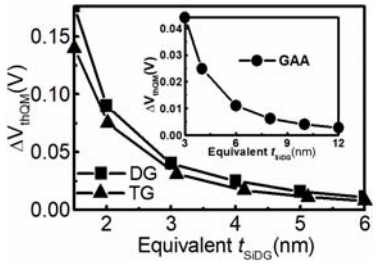
Figure 7 Variation of SS with the channel thickness for different MG MOSFETs



Note: Area of cross section of all devices are taken to be equal and t_{ox} = 1.5 nm.

Through the above discussion it is inferred that the silicon thickness should also be reduced with the reduction in channel length to have less SCE. However, Figure 8 shows the rise in threshold voltage when silicon thickness is reduced which is attributed to the QM effect. It is imperative to mention here that the comparative electrical characteristics of different gate structures is also affected by the choice of common channel-width (Figure 2) as reported in Jha and Choudhary (2018). Therefore, to get optimum performance from a device it is necessary to check the dependency of electrical characteristics on the physical parameters of the device.

Figure 8 Variation of threshold voltage of MG MOSFETs due to QM effects with equal area of cross sections, t_{ox} = 1.5 nm and L = 25 nm



4 Conclusions

The variation of SCEs in DG, TG and GAA MOSFETs by changing the device dimensions has been analysed. With the reduction in channel length, SCE increases and it

becomes more severe if the channel thickness is not reduced appropriately. It is observed that the most suitable candidate to extend the device scaling is GAA MOSFET. The advantage of our analysis is the use of simple yet efficient mathematical formulations for all device architectures and it also augurs well for the rapidly changing process technologies. As a further work, the impact of SCEs on the drain current of MG MOSFETs will be investigated.

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