Comparative performance analysis of FPGA-based MAC unit using non-conventional number system in TVL domain for signal processing algorithm

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Abstract: Today, the complication of binary digital hardware system is progressively growing. Due to this fact, new methodologies for efficiently describing and realising the digital systems are explored in this paper. Multi-valued logic methodology offers a few preferences over existing binary digital system. One of the well-known multi-valued logic systems is ternary value logic (TVL) system. It is seen that all kind of digital signal processing (DSP) algorithms widely use multiply-accumulate (MAC) operation for superior digital processing system. To implement high performance DSP algorithms MAC unit is used extensively. In current scenario, it is seen that non-conventional, non-binary number system-based architecture is also exhibited better performance. The example of such non-conventional, non-binary number systems is ternary residue number systems (TRNSs) and double base ternary number system (DBTNS). Here, a comparative study is made on performance analysis of MAC unit using various non-conventional, non-binary number system. All the architecture is mapped on FPGA for analysis its performance.

Keywords: ternary value logic; TVL; ternary residue number systems; TRNSs; TRNS adder; DBTNS; field programmable gate array; FPGA; DSP algorithms; multiply and accumulate unit; MAC; DBTNS multiplier.

Reference to this paper should be made as follows: Ghosh, A. and Sinha, A. (2020) 'Comparative performance analysis of FPGA-based MAC unit using non-conventional number system in TVL domain for signal processing algorithm', *Int. J. Nanoparticles*, Vol. 12, Nos. 1/2, pp.50–58.

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This paper is a revised and expanded version of a paper entitled 'FPGA implementation of RNS adder-based MAC unit in ternary value logic domain for signal processing algorithm and its performance analysis', presented at EDKCON, 2018 IEEE Electron Device Kolkata Conference, India, 24–25 November 2018.

1 Introduction

There is various type of numeral system present depending on the base. If the base is 3 then the numeral system is called ternary value logic (TVL) system (Hurst, 1984). Various studies showed its advantages over its binary counterpart. Some domain of binary numeral system like chip area, overall delay can be improved in TVL system (Sinha et al., 2006; Lin et al. 2011). Besides that, some literature showed the advantages of using non-conventional, non-binary number system like residue number systems (RNS) and double base number system (DBNS) for implementing various signal processing architecture (Ghosh et al., 2012a, 2012b; Roy et al., 2015; Chang et al., 2015; Chen et al., 2015). The advantages of non-conventional, non-binary number system are more lucrative when they are implemented in ternary domain. The basic advantages of ternary residue number systems (TRNSs) are the ability of performing carry-free addition operation, fault tolerant, detection and correction. TRNS can break one large number into smaller number depending on the moduli set (Ghosh and Sinha, 2018a). On the other hand, main advantage of double base ternary number system (DBTNS) lies in its ability of performing partial product-free multiplication operations (Ghosh and Sinha, 2018b). All digital signal processing (DSP) algorithms broadly utilise multiply-accumulate operation for the exclusive digital processing system (Singha et al., 2012; Seeta and Kumari, 2016). The multiplication and accumulation operations are prime operations of DSP algorithms. Thus, there is a demand for rapid processors having devoted hardware to upgrade the speed with which these multiplications and accumulations are performed. This operation facilitates the calculation of convolution which is required in various filter algorithms, Fourier transforms, etc. (Sinha et al., 2006). Basic modules of a MAC unit are a multiplier, an adder and an accumulator. The main challenge for a VLSI designer is to implement low power and high-throughput circuitry for high performance real-time DSP operations (Chen et al., 2015; Marzouqi et al., 2016; Karmakar and Karmakar, 2018). Effective implementation of a high performance MAC unit helps to perform efficient DSP operations. A partial product free multiplier can perform faster operation than conventional multiplier. So DBTNS multiplier can be an alternative. Again, carry-free adder can help to implement fast adder. So, TRNS adder can be a good solution. The main objective of this work is to study and compare the performance of multiplier and

accumulator (MAC) architectures in ternary domain using TVL, TRNS, DBTNS for realising various signal processing algorithms like finite impulse response (FIR) algorithm. The performance analysis of this architecture is executed and validated on Xilinx Virtex field programmable gate array (FPGA).

2 Brief analysis of various number system

TVL system is a non-binary multi-valued logic system. It mainly deals with three switching levels, i.e., denoted by 0, 1, 2. The arithmetic operations of TVL can deal with compliment operation, addition, subtraction, multiplication and division (Lin et al., 2011). The examples of non-conventional number system are TRNSs and DBTNS. A number can be broken in smaller number in TRNS domain depending on the moduli set and elements of moduli set should be mutually prime for getting better dynamic range. Suppose X is a number which is broken into N tuples, i.e., $X = (x1, x2, x3, \ldots, xN)$. Here $xi = X$ modulo mi, represents the i^{th} residue digit, mi is the i^{th} modulus and all mi are mutually prime numbers (Low and Chang, 2013; Matutino et al., 2015; Ghosh and Sinha, 2018a). An example of a balanced moduli set is $\{r^{n-2}, r^{n-1}, r^n\}$ where r signifies radix or base, for TVL domain the value of r is 3 (Abdallah and Skavantzos, 2005). Another non-conventional number system, DBTNS can help to represent a number as sum of mixed powers of two integer in ternary domain (Ghosh and Sinha, 2018b). For example, x is a ternary number then x can be expressed as follows:

$$x = \sum_{i,j} d_{i,j} 2^i 3^j$$

where $d_{ij} = \{0, 1, 2\}$. These indices (i, j) are in ternary number system.

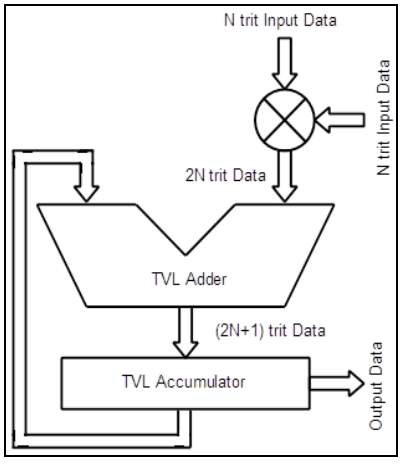
3 Architecture of MAC unit using various non-binary and non-conventional number system

A MAC unit which can able to perform single cycle multiplication and accumulation operation, is the one of the main modules of DSP processor (Ghosh et al., 2012b). So, MAC unit can help to implement DSP algorithms. Main modules of MAC unit are multiplier, adder and accumulator. The performance of MAC unit can be enhanced by improving the performance of basic modules of MAC unit, mainly multiplier and adder unit. The performance of MAC unit is enhanced by implementing basic modules of MAC unit in TVL, TRNS and DBTNS domain. The architecture of such MAC unit is discussed following sections.

3.1 Architecture of TVL-based MAC unit

The architecture of TVL-based MAC unit (Ghosh and Sinha, 2018b) is shown in Figure 1. It consists of multi-trit TVL Multiplier, multi-trit TVL adder and ternary register. Initially, N-trit inputs are stored in memory and fetched from a memory location and supplied to the multiplier unit for performing multiplication operation. The output of multiplier unit is $2N$ trit, so the output of the adder is of $2N + 1$. In this architecture, value of N is considered as 2 trit, 3 trit and 4 trit. In Figure 1, $x(n)$ and $h(n)$ are two N trit inputs and $y(n)$ is the final output of TVL MAC unit.

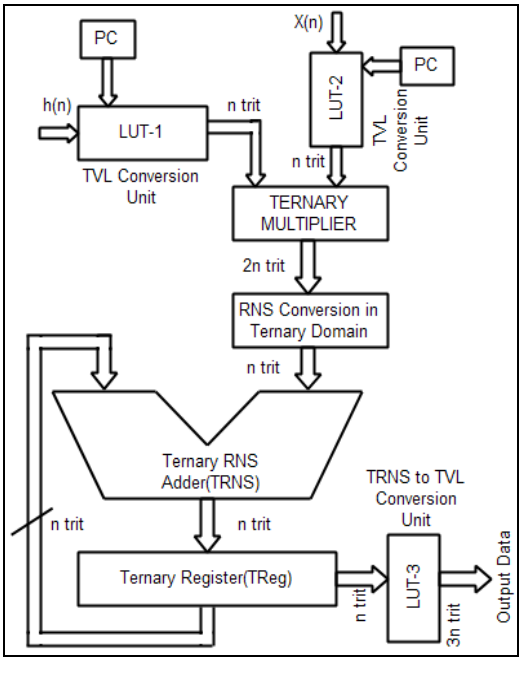
Figure 1 TVL-based MAC unit



3.2 Architecture of TRNS adder-based MAC unit

The architecture of TRNS adder-based MAC unit (Ghosh and Sinha, 2018a) is depicted in the Figure 2. The inputs of this architecture of MAC unit are in TVL. Initially, two inputs [in Figure 2, $x(n)$ and $h(n)$ are the inputs of n trit) are multiplied in TVL domain. Then the TVL-based product is converted in TRNS to perform the carry-free addition in TVL domain. Basic modules of this TRNS Adder-based MAC unit are TVL conversion, TVL multiplier, TVL – RNS conversion, TRNS adder, ternary registrar (TReg).

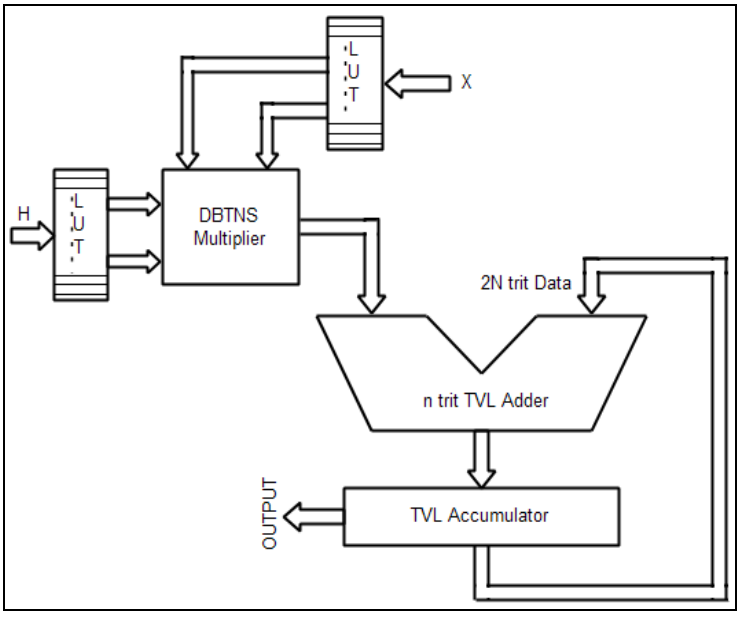
Figure 2 TRNS adder-based MAC unit



3.3 Architecture of DBTNS multiplier-based MAC unit

The architecture of DBTNS multiplier-based MAC unit (Ghosh and Sinha, 2018b) is depicted in Figure 3. In this architecture, two inputs $h(n)$ and $x(n)$ which are in TVL domain elements, are converted into DBTNS. The basic modules of such architecture are TVL conversion, DBTNS conversion, DBTNS multiplier, TVL adder, ternary registrar (accumulator). Initially, $x(n)$ and $h(n)$ are represented into DBTNS, i.e., $x(n) = 2^{i_1}.3^{j_1}$ and $h(n) = 2^{i_2}.3^{j_2}$. The indices of 2 and 3 are fed through DBTNS multiplier unit and multiplied data is added with zero which is initially stored in an accumulator. The trit length of indices i and j are considered as 1, 2, 3 then trit length of output becomes 7, 27, 85 respectively.

Figure 3 DBTNS multiplier-based MAC unit



4 Comparative performance analysis of MAC unit

FIR filter algorithm (Chen et al., 2015) is implemented using non-binary and non-conventional number system-based MAC unit. The delay and hardware complexity (Ghosh and Sinha, 2018b) of TVL MAC unit-based FIR filter is defined as the total delays of different modules. Total delay of this FIR filter = (n-trit LUT access delay + time taken by TVL multiplier + time taken by TVL adder). Total delay of n-trit TVL adder = (THA + (n – 1) . Tc), where, THA is time taken by half adder and Tc is the carry propagation delay in later stages. The time complexity (Ghosh and Sinha, 2018a) of TRNS MAC unit-based FIR filter depends on the basic modules like TVL conversion unit, ternary multiplier unit, TRNS conversion unit, TRNS adder unit and ternary registrar unit. The total delay of FIR filter using TRNS MAC unit can be represented as

(*n*-trit LUT access time for integer to TVL conversion + time taken by ternary multiplier unit + time taken by TRNS conversion + time taken by TRNS adder + *n*-trit LUT access time for TVL to integer conversion). TRNS conversion unit is implemented using ternary ripple carry adder (RCA) and ternary multiplexer. So the time taken by TRNS conversion unit can be calculated as (time taken by *n*-trit ternary RCA + time taken by ternary multiplexer). TRNS adder unit is implemented using ternary RCA, ternary subtractor and ternary multiplexer and de-multiplexer. So time taken by TRNS adder unit can be calculated as (time taken by *n*-trit ternary RCA + time taken by ternary de-multiplexer + time taken by *n*-trit ternary subtractor + time taken by ternary multiplexer). The total delay of FIR filter using DBTNS MAC unit can be represented as (*n*-trit LUT access time for integer to TVL conversion + *n*-trit LUT access time for TVL to DBTNS conversion + time taken by DBTNS multiplier + time taken by TVL adder + *n*-trit LUT access time for TVL to integer conversion). If the number of trit of indices of input data of FIR filter (Chen et al., 2015; Chang et al., 2015) are changed then execution time is also varied. Synthesis report of eight tap FIR filter with change of trit is shown in following tables. Tables 1, 2 and 3 represent the synthesis report of TVL, TRNS, DBTNS MAC unit-based FIR filter respectively.

The hardware complexity of the non-conventional MAC unit-based FIR filter is represented by Figures 4 and 5. Figure 4 represents the relation between number of LUTs and number of input trit and Figure 5 represents the relation between input trit and execution time.

Table 1 Synthesis report of eight tap FIR filter using TNS MAC unit with change of trit

Sl. no.	*No. of trit*	*Synthesis report*			
		Number of slice LUTs	*Minimum period*	*Minimum input arrival time before clock*	*Maximum output required time after clock*
1	4	148 out of 46,560	3.571 ns (maximum frequency: 279.994 MHz)	6.464 ns	0.576 ns
2	3	84 out of 46,560	2.853 ns (maximum frequency: 350.471 MHz)	4.974 ns	0.576 ns
3	2	35 out of 46,560	2.135 ns (maximum frequency: 468.362 MHz)	3.066 ns	0.576 ns

Table 2 Synthesis report of eight tap FIR filter using TRNS MAC unit with change of trit

Sl. no.	*Input data trit length (n)*	*Moduli set*	*Synthesis report*			
			Number of slice LUTs	*Minimum period*	*Minimum input arrival time before clock*	*Maximum output required time after clock*
1	2	{7, 8, 9}	126 out of 46,560	2.013 ns (maximum frequency: 496.697 MHz)	6.107 ns	0.618 ns
2	3	{25, 26, 27}	232 out of 46,560	2.439 ns (maximum frequency: 410.071 MHz)	9.492 ns	0.609 ns
3	4	{79, 80, 81}	382 out of 465,607	2.775 ns (maximum frequency: 360.386 MHz)	12.490 ns	0.604 ns

Table 3 Synthesis report of eight tap FIR filter using DBTNS MAC unit with change of trit

Sl. no.	*Input index trit length (i, j)*	*Synthesis report*			
		Number of slice LUTs	*Minimum period*	*Minimum input arrival time before clock*	*Maximum output required time after clock*
1	1	90 out of 343,680	6.405 ns (maximum frequency: 156.128 MHz)	8.098 ns	0.676 ns
2	2	308 out of 343,680	11.996 ns (maximum frequency: 83.364 MHz)	14.235 ns	0.676 ns
3	3	619 out of 343,680	21.887 ns (maximum frequency: 45.690 MHz)	25.736 ns	0.676 ns

Figure 4 Complexity analysis of eight-tap FIR filter using non-binary and non-conventional number system-based MAC unit with the change of trit for input trit vs. number of slice LUTs (see online version for colours)

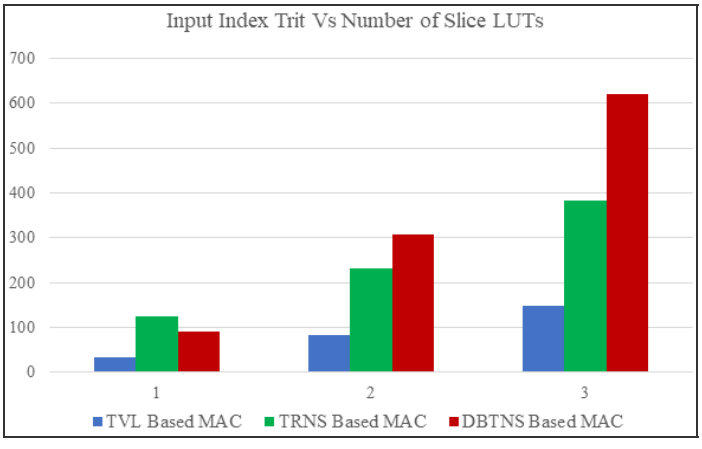
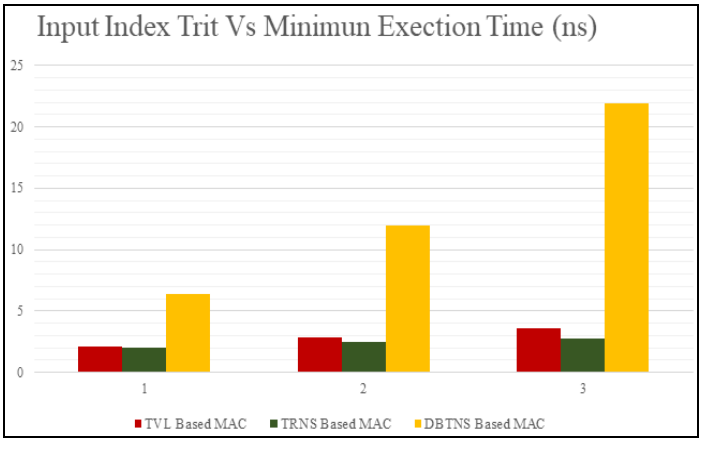


Figure 5 Complexity analysis of eight-tap FIR filter using non-binary and non-conventional number system-based MAC unit with the change of trit for input trit vs. minimum execution time (ns) (see online version for colours)



5 Conclusions

The non-convention number system offers several benefits over existing binary digital system (Ghosh et al., 2012b; Roy et al., 2015; Ghosh and Sinha, 2018a). This paper deals with comparative study of non-conventional number system-based MAC unit for implementing eight-tap FIR filter. The basic advantages of using TVL system are its capabilities to reduce chip area, reduce overall delay over conventional binary number system. TRNS offers a promising feature that is carry-free operations in addition, subtraction and multiplication. The complexity of calculation in many applications, such as encryption and fuzzy systems can be reduced by this integral property of TRNS. On the other hand, an efficient multiplier can be implemented by DBTNS. It can help to reduce the complexity of multiplication. All the architectures were validated on Xilinx FPGA (Dabhade et al., 2018) and the detailed analysis and studies of different modules of the non-conventional MAC units have been simulated using Xilinx ISE version 12.3. The novelty of the architecture of MAC unit is justified by analysing the experimental results. A comparative study can also be made on other fast and high end signal processing-based applications (Armah and Ahene, 2015; Marzouqi et al., 2016; Karmakar and Karmakar, 2018) like high quality image processing, audio, speech, and language processing systems, acoustic echo suppression (AES) and acoustic echo cancellation (AEC), and more rarely line echo cancellation (LEC), etc. Non-conventional mixed radixes-based MAC architecture for signal processing algorithm can also be a topic of discussion for researchers. Beside that reconnoitring the opportunities of VLSI implementation of the multi-valued logic system using TRNS-DBTNS mixed base can also be a topic for future work.

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