GaAs SOI FinFET: impact of gate dielectric on electrical parameters and application as digital inverter

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Abstract: In this paper, a GaAs SOI (silicon on insulator) FinFET is proposed. A comparative study between proposed GaAs FinFET and conventional Si FinFET is presented. The effects of dielectric constant (k) of gate dielectric material on electrical parameters like channel potential, drain current, and \( I_{\text{on}}/I_{\text{off}} \) have been reported. Results show that as k raises, both \( I_{\text{on}}/I_{\text{off}} \) and channel potential increases. Again the impact of k on short channel effects (SCEs) has been investigated. TCAD results show that as k increases subthreshold swing (SS) improves, drain induced barrier lowering (DIBL) degrades, and \( V_{T} \) roll off occur. The impacts of k on gate capacitance (\( C_{GG} \)) and intrinsic delay (\( \tau \)) have been presented and they increases as k increases. A digital CMOS inverter is implemented through proposed FinFET and the effect of k on its delay parameter is estimated. Results shows that average delay increase as k increases.

Keywords: CMOS inverter; dielectric constant; FinFET; GaAs; SOI.


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1 Introduction

Over the years, the continuous downscaling of device dimensions, has degraded the performance of MOSFETs which lead to various short channel effects (SCEs) like high subthreshold swing (SS), high drain-induced barrier lowering (DIBL) and threshold voltage (V\textsubscript{T}) roll-off (Bhattacharya and Jha, 2014; Roy et al., 2003). The scaling of oxide thickness results in gate induced drain leakage (GIDL) (Orouji and Rahimian, 2012; Yeo et al., 2003). But in order to follow the Moore’s law we have scaled the device dimensions (Moore, 1965). To overcome these problems researcher have proposed various device architectures. Among different device structure, FinFET is a promising candidate, as it can control the channel from all the three side of the gate (Bhattacharya and Jha, 2014; Fasarakis et al., 2012). A MOSFET with Si fin as a vertical channel is named as FinFET. To further expand the performance of FinFET, researcher has recognised various new technologies such as modification in structure, SOI FinFET, channel materials beyond silicon such as Ge or groups 3–5 semiconductor, high-k/metal gate stack, and heterojunction FinFET. SOI FinFET has some inherent properties like it provides high drive current, high mobility, less delay, and minimises the leakage current (Narendar and Mishra, 2015; Ritzenthaler et al., 2010; Tang et al., 2001; Yeh et al., 2013). Again to have more controllability on the channel the high k dielectric materials are considered as promising gate dielectric (Narendar and Mishra, 2015). In Chau et al. (2004), high-k dielectric material (HfO\textsubscript{2}) is used to improve the electrical performance for both NMOS and PMOS device. In Ortiz et al. (2010), the channel is surrounded by zirconium dioxide which leads to decreasing the power consumptions and improve the device performance. Some other researcher also used high-k as gate dielectric to improve the performance of the device (Chatterjee et al., 2015; Chau et. al., 2004). But, the effect of dielectric constant in GaAs FinFET semiconductor has not yet been reported. However, different electrical parameters such as V\textsubscript{T}, carrier mobility, drive current etc. are a function of dielectric constant of gate dielectric. Therefore, investigation on the effect dielectric constant of gate dielectric on electrical parameters is necessary. In this paper, the impact of dielectric constant of gate oxide on various electrical parameters is investigated in GaAs SOI FinFET. A CMOS inverter is implemented with proposed device and the effect of dielectric constant on its properties also discussed. Furthermore, a comparison of GaAs SOI FinFET with silicon FinFET is presented.

The rest of the paper is organised as follows. Sections 2 demonstrate the device structure and simulation methodology. Results and discussion are discussed in Section 3. Finally, summary of the work is concluded in Section 4.
The 3D and 2D view of the proposed GaAs SOI FinFET used in this work are shown in Figure 1(a) and 1(b), respectively. The fin of the proposed device is made of GaAs. SiO\textsubscript{2} acts as buried oxide. Gate polysilicon is used as gate material. The doping concentration of n\textsuperscript{+} source, n\textsuperscript{+} drain, and p-type channel region are 10\textsuperscript{19}, 10\textsuperscript{19} and 10\textsuperscript{16} cm\textsuperscript{-3}, respectively. On doing simulation, the value of work function of gate material and VDS are considered as 4.6 eV and 0.5 V, respectively. The dimensions of the device with their symbols as indicated in Figure 1(b) are listed in Table 1. The length of source/drain region is 7 nm, which is not listed in Table 1.

**Table 1** Dimensions of various parameters for proposed structure

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buried oxide thickness (A)</td>
<td>18</td>
</tr>
<tr>
<td>Buried oxide height (B)</td>
<td>20</td>
</tr>
<tr>
<td>Fin width (W\textsubscript{fin})</td>
<td>12</td>
</tr>
<tr>
<td>Fin height (H\textsubscript{fin})</td>
<td>30</td>
</tr>
<tr>
<td>Gate oxide thickness (t\textsubscript{ox})</td>
<td>2</td>
</tr>
<tr>
<td>Gate metal thickness (M)</td>
<td>1</td>
</tr>
</tbody>
</table>

Simulation of the proposed GaAs SOI FinFET has been carried out on Sentaurus Technology Computer Aided Design (TCAD) tool (TCAD User Guide, 2011). As highly doped source and drain region are present, Fermi-Dirac distribution (TCAD User Guide, 2011) and bandgap narrowing model are activated in our simulation. To consider the effect of mobility the Phonon mobility model is enabled in our simulation (TCAD User Guide, 2011). SRH is activated to consider the recombination generation in simulation.
3 Results and discussion

In this section, a comparative study between proposed device and conventional FinFET (C-FinFET) is investigated. The impact of dielectric constant of gate dielectric on various parameters like drain current, surface potential, SCEs, gate capacitance, intrinsic delay, and transconductance for channel length \( L_g = 16 \) nm of GaAs SOI FinFET is discussed. Impact of dielectric constant of gate dielectric on inverter characteristic in GaAs SOI FinFET is also examined. The gate dielectric materials with their dielectric constant considered in this work are: SiO\(_2\) \((k = 3.9)\), Si\(_3\)N\(_4\) \((k = 7.5)\), Al\(_2\)O\(_3\) \((k = 10)\), and HfO\(_2\) \((k = 24)\).

3.1 Comparison of proposed device with conventional FinFET

Figure 2 depicts the comparison of drain current between conventional and GaAs SOI FinFET in log scale. The dimension of C-FinFET is same as proposed device, except the fin material is made of Silicon. A lower value of off current is obtained with insignificant degradation in on current for proposed FinFET compared to C-FinFET and this is due to high band gap of GaAs. The proposed device has SS value of 63.21 mV/dec. whereas for C-FinFET SS is 65.54 mV/dec. Because of these advantages the analysis on effect of dielectric constant of gate dielectric has been carried out in proposed device.

Figure 2 Comparison of drain current between proposed and C-FinFET (see online version for colours)

3.2 Effect of dielectric constant of gate dielectric on potential, drain current and SCEs

Figure 3(a) shows the variation of surface potential at different dielectric constant \( k \) for the proposed device. It is observed that with the increase of \( k \) the potential along the channel also increases and this is due to increase in gate controllability at higher value of \( k \).
The variation of drain current at different k of gate dielectric is shown in Figure 3(b) and 3(c) in log and linear scale, respectively. It is observed that drain current decreases and increases in linear and saturation region as summarised in Figure 3(b) and 3(c), respectively. With increase in k gate controllability over the channel increases which increases the inversion charge in the channel and leading to increase in on current. However, in linear region drain current decreases with increase in k and this is due to the presence of depletion capacitance with inversion capacitance in weak inversion region which reduces gate control with k. Therefore, off current decreases with k.

The value of SS decreases with increase in k as shown in Figure 4(a). As k increases, the gate control over the channel improves and which results in decrease in SS value. SS can be expressed according to equation (1) (Tsividis and McAndrew, 2011).

\[ SS = 2.3\eta V_T \]  

where \( V_T \) is thermal voltage and \( \eta \) is subthreshold slope is given by (Tsividis and McAndrew, 2011):

\[ \eta = 1 + \frac{C_{dep}}{C_{ox}} \]
where $C_{\text{dep}}$ and $C_{\text{ox}}$ are depletion and oxide capacitance, respectively. $C_{\text{ox}}$ is given by

$$C_{\text{ox}} = \frac{k}{t_{\text{ox}}}$$

where $k$ and $t_{\text{ox}}$ are respectively dielectric constant and oxide thickness of gate dielectric. It is seen from equation (3) that as $k$ increases $C_{\text{ox}}$ increases which results in decrease in $\eta$ and lead to reduction in SS. A SS of 67.8 mV/dec. has obtained at $k = 24$.

**Figure 4** Effect of dielectric constant of gate dielectric on (a) SS and DIBL (b) $I_{\text{on}}/I_{\text{off}}$ and $V_T$

DIBL is one of the critical parameter that affects the performance of the device vary detrimentally (Naderi et al., 2012). The value of DIBL increases with increase in $k$ of gate dielectric material. DIBL effect occurs when barrier height at source side decreases under the application of high drain voltage and as a result channel is controlled by drain instead of gate. Similar mechanism is observed with increase of $k$ of gate dielectric material which results in increase of DIBL as shown in Figure 4(a).

The most significant parameters for nanoscale device are $V_T$ and $I_{\text{on}}/I_{\text{off}}$. The value of $I_{\text{on}}/I_{\text{off}}$ increases and $V_T$ decreases with the increase in $k$ of gate dielectric as portrayed in Figure 4(b). It is seen from Figure 4(b) and 4(c) that with increase of $k$ the value of off current ($I_{\text{off}}$) in linear region decreases and on current ($I_{\text{on}}$) increases in superthreshold region, which this results in improvement in $I_{\text{on}}/I_{\text{off}}$.

The $V_T$ can be defined as (Colinge, 2008):

$$V_T = \varphi_{ms} + 2\varphi_F + \frac{Q_D}{C_{\text{ox}}}$$

where $Q_D$ is depletion charge in the channel, $\varphi_{ms}$ is metal semiconductor work function difference, $\varphi_F$ is Fermi potential. For p-type semiconductor $\varphi_F$ can be expressed as:

$$\varphi_F = \left(\frac{KT}{q}\right)\ln\left(\frac{N_A}{n_i}\right)$$

where $K$ is Boltzmann constant, $T$ is temperature, $q$ is electronic charge, $N_A$ is acceptor concentration in p-type body, and $n_i$ is intrinsic carrier concentration. By substituting equation (3) in equation (4), it can be summarised that as $k$ increases $C_{\text{ox}}$ decreases which lead to reduction in $V_T$. 

3.3 Effect of dielectric constant of gate dielectric on transconductance, gate capacitance and intrinsic delay

Figure 5(a) shows the variation of transconductance with gate voltage as a function of $k$ of gate dielectric. The transconductance is defined as the variation in drain current due to change in gate source voltage at fixed drain to source voltage. Transconductance ($g_m$) can be expressed as equation (4) (Balamurugan et al., 2009).

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$  \hspace{1cm} (6)

where $I_D$ and $V_{GS}$ are respectively drain current and gate to source voltage. It is observed that transconductance increases with increase in $k$ and this is due to enhancement of gate control over the channel with $k$. A peak value of $g_m$ is observed at $V_{GS} = 0.75$ V.

The dielectric constant ($k$) of gate dielectric has prominent effect on gate capacitance ($C_{GG}$) and it is seen that $C_{GG}$ increases as $k$ increases as shown in Figure 5(b). This is because as $k$ increases gate control enhance which reduces the energy bandgap and leads to increase in flow of charge into the channel. The amounts of charge carrier in channel increases and in order balance the charge, the gate charge also increases. As expected with increase of gate charge the gate capacitance also increases. With increase in $C_{GG}$
with $k$, gate control over the channel improves which leads to improvement in the drain current and therefore, on current increases with $k$. Again from Figure 5(b), it is visualised that as gate voltage increases, $C_{GG}$ increases. This is because increase in gate bias increases the amount of charge on gate which leads to increase in gate capacitance.

The impact of $k$ on intrinsic delay is depicted in Figure 5(c). The intrinsic delay ($\tau$) is given by equation (7) (Rai et al., 2012).

$$\tau = C_{GG} \times \frac{V_{DD}}{I_{on}}$$  \hspace{1cm} (7)

From Figure 5(b) and 3(c) it is visualised that, as $k$ increases both $C_{GG}$ and $I_{on}$ increases, respectively. But increase in $C_{GG}$ is more significant than $I_{on}$ and at $V_{DD} = 0.5$ V, therefore the intrinsic delay also increase. It is also observed from Figure 5(c), as $C_{GG}$ increases with $V_{GS}$, the amount of delay also increases.

Table 2 Comparative study of proposed FinFET with other reported results at $k = 10$

<table>
<thead>
<tr>
<th>Electrical parameters</th>
<th>Proposed FinFET</th>
<th>Ref. (Ritzenthaler et al., 2010)</th>
<th>Ref. (Rai et al., 2012)</th>
<th>Ref. (Yu et al., 2002)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS (mV/dec)</td>
<td>72.4</td>
<td>92</td>
<td>64.2</td>
<td>78</td>
</tr>
<tr>
<td>$I_{on}/I_{off}$</td>
<td>$4.48 \times 107$</td>
<td>$8.89 \times 105$</td>
<td>$1.33 \times 106$</td>
<td>1.42</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>50.81</td>
<td>197</td>
<td>55</td>
<td>37</td>
</tr>
<tr>
<td>$C_{GG}$ (fF)</td>
<td>0.0021</td>
<td>N/A</td>
<td>0.0324</td>
<td>1200</td>
</tr>
<tr>
<td>Intrinsic delay (psec)</td>
<td>0.0118</td>
<td>N/A</td>
<td>4</td>
<td>1.2</td>
</tr>
<tr>
<td>Transconductance ($\mu$S$/$$\mu$m)</td>
<td>46,666</td>
<td>N/A</td>
<td>N/A</td>
<td>820</td>
</tr>
</tbody>
</table>

The electrical parameters of proposed device for $k = 10$ is compared with other existing work as summarised in Table 2. From Table 2, it can be conclude that proposed FinFET has lower SS, higher $I_{on}/I_{off}$, lower $C_{GG}$, lower delay, lower DIBL and higher transconductance than other reported literature.

3.4 Effect of dielectric constant of gate dielectric on inverter characteristic

In this section, a CMOS digital inverter is designed through TCAD simulator using the proposed GaAs SOI FinFET at channel length 16 nm and the delay parameters are calculated. Figure 6(a) shows the pictorial view of digital inverter and a load capacitor $C_L$ is used at output. The optimised value of $C_L$ is 0.3 fF. The drain current vs. gate voltage characteristic for both P-GaAs FinFET and N-GaAs FinFET is portrayed in Figure 6(b). A close $I_{on}/I_{off}$ ratio is obtained for both N-FinFET and P-FinFET. The input and output voltage level at different $k$ is shown in Figure 7. It is observed from output waveform that the proposed device has negligible amount of undershoot as well as overshoot. However, undershoot and overshoot reduces with increase in $k$. This is because increase in $k$ enhances the gate control leads to increase in gate capacitance. Gate capacitance is inversely proportional with overshoot and undershoot (Goswami et. al., 2016), which leads to decrease in overshoot and undershoot with $k$. The delay parameters are
calculated from Figure 7 and are stated in Table 3. The value of time takes to output fall from high to low ($t_{\text{pHL}}$) is more compared to time takes to output rise from low to high ($t_{\text{plH}}$) which is in consistent with literature (Han et. al., 2013). It is seen from Table 3 that average delay increases with $k$ and this is due to increase in $C_{\text{GG}}$ with $k$. As $k$ increases digital circuit delay increases and $I_{\text{on}}/I_{\text{off}}$ reduces [Figure 4(b)], and therefore there is tradeoff between delay and $I_{\text{on}}/I_{\text{off}}$. Hence, $k = 7.5$ is favourable, as $I_{\text{on}}/I_{\text{off}}$ in order of 108 with average delay 1.75 psec.

Figure 6 (a) Implementation of CMOS Inverter using proposed device (b) Transfer characteristic of P-FinFET and N-FinFET (see online version for colours)
Figure 7  Transient characteristic of the CMOS GaAs-FinFET inverter at different dielectric constant of gate dielectric (see online version for colours)

Table 3  Delay parameters at different k for proposed structure

<table>
<thead>
<tr>
<th>Delay parameter</th>
<th>k = 3.9</th>
<th>k = 7.5</th>
<th>k = 24</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{pLH}} ) (psec)</td>
<td>0.3</td>
<td>0.4</td>
<td>0.7</td>
</tr>
<tr>
<td>( t_{\text{pHL}} ) (psec)</td>
<td>3</td>
<td>3.1</td>
<td>3.2</td>
</tr>
<tr>
<td>Average delay (psec)</td>
<td>1.65</td>
<td>1.75</td>
<td>1.95</td>
</tr>
</tbody>
</table>

Table 4  Comparison of inverter performance of proposed structure with Ref. (Rai et al., 2012) at \( k = 3.9 \).

<table>
<thead>
<tr>
<th>Delay parameter</th>
<th>Proposed FinFET</th>
<th>Ref. (Rai et al., 2012)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{pHL}} ) (psec)</td>
<td>3</td>
<td>2.37</td>
</tr>
<tr>
<td>( t_{\text{pLH}} ) (psec)</td>
<td>0.3</td>
<td>1.17</td>
</tr>
<tr>
<td>Average delay (psec)</td>
<td>1.65</td>
<td>1.77</td>
</tr>
</tbody>
</table>

The delay parameters for proposed GaAs FinFET are compared with Ref. (Rai et al., 2012). It is observed that proposed GaAs FinFET has less value of intrinsic delay. Therefore, proposed device has better switching characteristic.

4 Conclusions

The influence of varying dielectric constant (k) of gate dielectric on drain characteristic, channel potential, \( V_T \), \( I_{\text{on}}/I_{\text{off}} \), SS, DIBL, transconductance, gate capacitance, and intrinsic delay have been reported in a GaAs SOI FinFET. It is noticed that as k increases the drain current improves both in linear and superthreshold region, and the channel potential also increases. Moreover, it is observed that increasing k leads to improvement in SCEs and high \( I_{\text{on}}/I_{\text{off}} \). The value of transconductance and intrinsic delay of the device increases as k increases. The k affects the delay parameters of a digital inverter and it is perceived that average delay increases with increase in k. Therefore, such investigation will be advantageous for design consideration of this device.
References

