A comparative study on the effects of technology nodes and logic styles for low power high speed VLSI applications

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Abstract: Carbon nanotubes (CNT) field-effect transistor (CNTFET) could be a possible alternative to CMOS technology for future VLSI applications. In this work, a comparative study has been carried out on the effects of technology nodes and logic styles on power dissipation, delay, leakages, etc. The technology nodes that are considered here are 90 nm and 32 nm MOSFET technology, and 32 nm CNTFET technology. The logic families considered here are the conventional complementary metal-oxide-semiconductor (CMOS), complementary pass transistor logic (CPL) and transmission gate (TG). The digital circuits considered are NAND, NOR, XOR and MUX gates. HSPICE simulations have been carried out and observed that at 32 nm CNTFET technology, the least power, worst-case delay and least PDP are found as 15.5 nW, 3.11 ps and 0.048 aJ, respectively. It is witnessed that CNTFET-based logics are superior compared to other logic families at different technology nodes.

Keywords: logic styles; complementary metal oxide semiconductor; CMOS; complementary pass transistor logic; CPL; transmission gate; TG; power delay product; PDP; CNTFET.

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1 Introduction

The main emphasis today in the field of VLSI design is to enhance the speed and reduce power consumption (Chandrakasan et al., 2003). There are stringent design constraints such as small area, high speed and low power circuitry and low cost for portable consumer applications (Anis et al., 2002; Hussain et al., 2019). Therefore, it becomes the major concern for the designer to implement digital circuits and systems for high speed of operation with low power consumption (Hussain and Chaudhury, 2018; Hussain and Kumar, 2017a).

As conventional MOSFET technology is called down to deep nanometre level, there are critical challenges and difficulties. Key design challenges today are short channel effects, increased leakage currents, reduced gate control, severe process variations, high power densities, etc. Because of all these constraints, it is very challenging to design and implement high-performance circuit and systems. This has led to the design and development of new devices and technologies for the next-generation semiconductor technologies. As the VLSI technology trend progresses into an era of nanotechnology, different molecular devices (Avouris et al., 2007) such as FinFET (Kim and Roy, 2004), tunnel FET (TFET), single electron transistor (SET) (Durrani et al., 2009), carbon nanotubes field effect transistor (CNTFET), etc. are becoming an alternative to the existing complementary metal oxide semiconductor (CMOS) technology. These devices are also growing very fast, and it is obvious that these new devices may succeed the existing bulk-Si-CMOS technology in coming days. CNTFET shows more potential amongst other emerging device technologies. CNTFET has many advantages and suitable for circuit applications as compared to other technology based on Si/Ge (Deng and Wong, 2007a). CNTFET can easily replace Si-based CMOS technology as its working concept and the operational structure is similar to later. With the intrinsic attributes and one-dimensional unique band structure, CNTFET could be more useful than other technologies (Deng and Wong, 2007b; Hussain and Chaudhury, 2019). CNTFETs are found to be faster and have less leakages, then other bulk-Si transistor technologies (McEuen et al., 2002; Hussain et al., 2019). Hence, the suitability of CNTFETs in high-performance applications is more. The increasing demand of CNTFET technology over CMOS technology is due to the easier transistor sizing as it has the same size and

mobility for p-CNTFET and n-CNTFET which lead to same current drive capabilities, whereas in CMOS both PMOS and NMOS are needed to be sized individually (Javey et al., 2004).

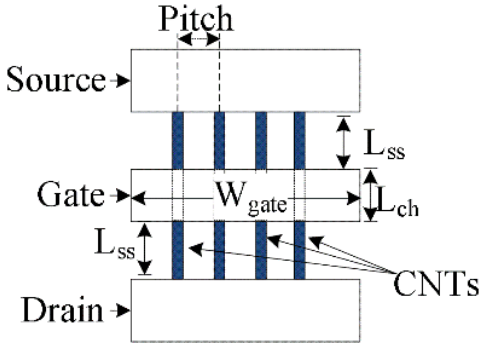
Similarly, as the technology scales down, power consumption, delay, gate capacitance, etc. varies accordingly (O'Connor et al., 2007). Therefore, the choice of a proper logic is also a prominent factor in enhancing the speed and for reduced power consumption (Sanjeet and Chaudhury, 2013). In this paper, the effects of different technology on logic styles for various design metrics are observed. Here, CMOS and complementary pass transistor logics (CPLs) are utilised to design the basic digital gates, e.g., NAND gate, NOR gate, XOR gate and multiplexer (MUX) circuit. These circuits are implemented in 90 nm and 32 nm bulk-Si-CMOS technology and using 32 nm MOSFET-like CNTFET technology. With nominal operating conditions, power, delay and power delay product (PDP) are investigated.

The organisation of this paper is as follows. Section 2 explores a detailed review about CNTFET, in Section 3, discussion on logic style, and in Section 4 discusses the design constraints and test bench. In Section 5, the performance analysis and discussion are given. Section 6 concludes this paper.

2 Overview of CNTFET devices

Carbon nanotubes (CNT) are made from graphite. CNT is formed by rolling-up a graphite sheet over a wrapping vector (m, n), where (m, n) is known chirality of CNT. CNTs are of two types and they are categorised based on types of the wall they pose as single-walled-carbon-nanotube (SWCNT) and multi-walled-carbon-nanotube (MWCNT) (Hussain and Kumar, 2017b). SWCNTs can be metallic or semiconducting and their chirality vector decides the type (O'Connell, 2006; Martel et al., 2001). In CNTFETs, the channel uses semiconducting type SWCNT, the numbers may vary from one to many (Vaddi et al., 2010). The schematic diagram of the CNTFET is shown in Figure 1.

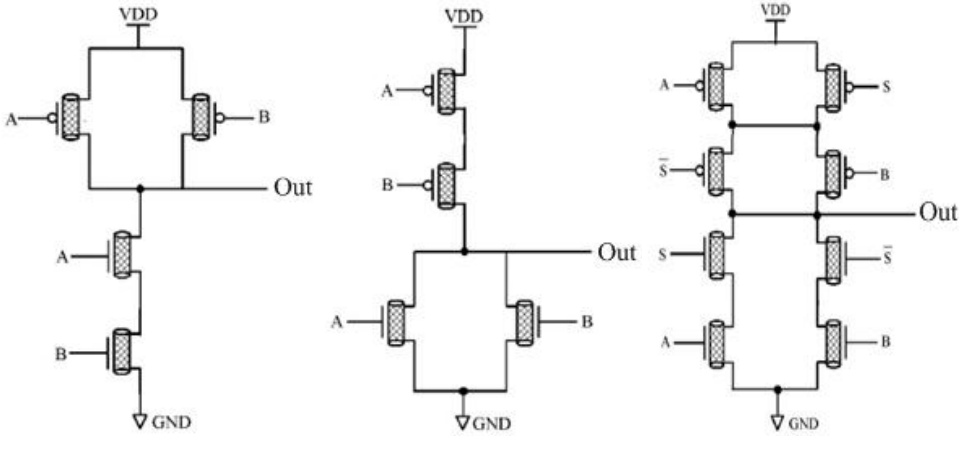
Figure 1 Schematic of CNTFET (see online version for colours)



There are different types of CNTFET devices are there such as SB-CNTFET, T-CNTFET, MOSFET like CNTFET, etc. MOSFET like CNTFETs devices are much more stable with higher on/off ratios (Ion/Ioff) as compared to the SB-CNTFETs (Chau et al., 2005). It operates based on the potential applied to the gate. It also shows unipolar characteristics. On the merit of these advantages, MOSFET-like CNTFETs are very appropriate for high-performance applications. It also shows similarity with MOSFETs in terms of operation and characteristics. In this paper, MOSFET like CNTFET is used for the implementation, and so now onwards in this paper the word CNTFET. The different parameters of CNTFET are the size of CNTFET, the threshold voltage (V_{th}), on-off current ratio, trans-conductance (g_{cnfet}), sub-threshold slope (SS), gate delay (t_d) and switching energy (E_{dyna}) (Javey et al., 2004).

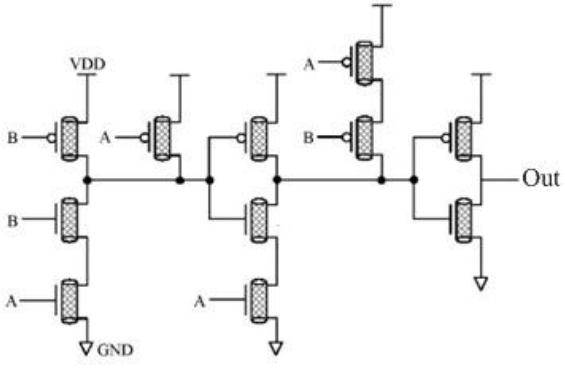
For simulation, the CNTFET model used is offered by Stanford University (https://nano.stanford.edu/stanford-cnfet-model/). In this standard 32 nm CNTFET model, the type of CNTFT considered is MOSFET-like CNTFET, where CNTs are used as shown in Figure 1 (Hussain and Chaudhury, 2019). This CNTFETs have multi-channels with high-k gate material. The source and drain regions of the model are heavily doped whereas the CNT channel region is intrinsic (Deng and Wong, 2007a). A compact PICE model has been released considering different issues like device non-idealities, elastic scattering, parasitic capacitance, resistance at the interference between the metal contact and doped CNT as well as the quantum/series resistance are considered (Deng and Wong, 2007b). Here, flexibility is given to the designer to choose a transistor with one or more CNTs. Some of the important design parameters of CNTFET are Lch (physical channel length), the mean free path in the intrinsic CNT channel, the length of the doped CNT source-side extension region, the dielectric constant of the high-k top gate dielectric material and the thickness of the high-k top gate dielectric material. The model can be used for SPICE simulations for circuits and systems (Hussain and Chaudhury, 2019).

Figure 2 (a) CMOS-based NAND gate, (b) CMOS-based NOR gate, (c) CMOS-based MUX and (d) CMOS-based XOR gate



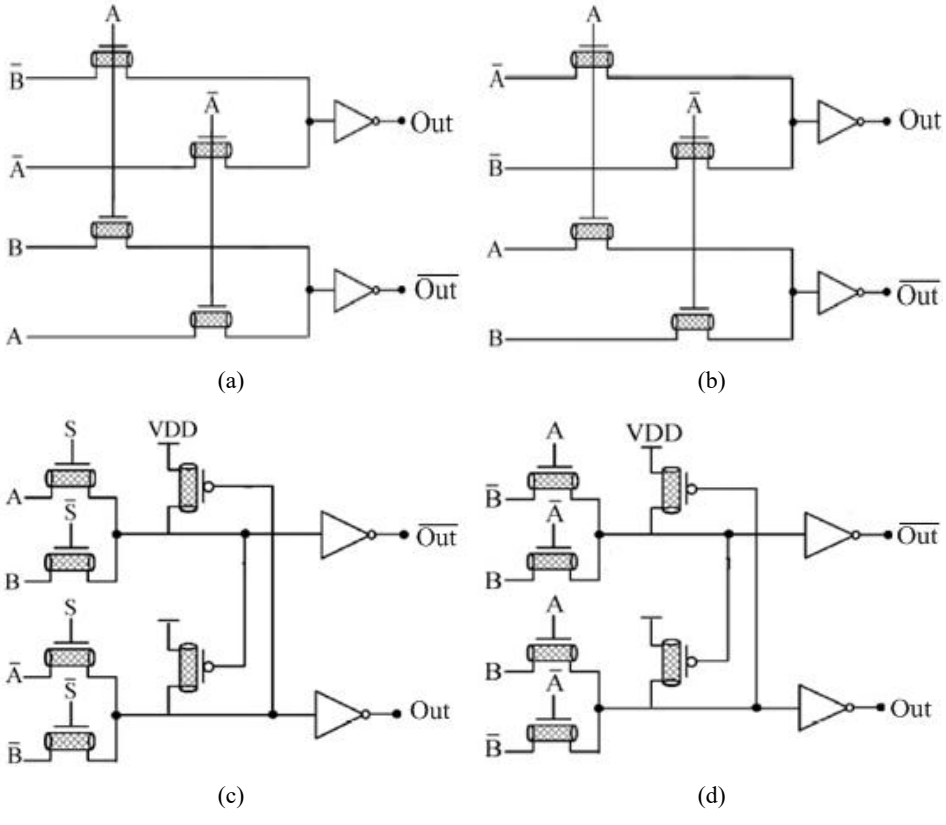
(a) (b) (c)

Figure 2 (a) CMOS-based NAND gate, (b) CMOS-based NOR gate, (c) CMOS-based MUX and (d) CMOS-based XOR gate (continued)



(d)

Figure 3 (a) CPL-based NAND gate, (b) CPL-based NOR gate, (c) CPL-based MUX and (d) CPL-based XOR gate

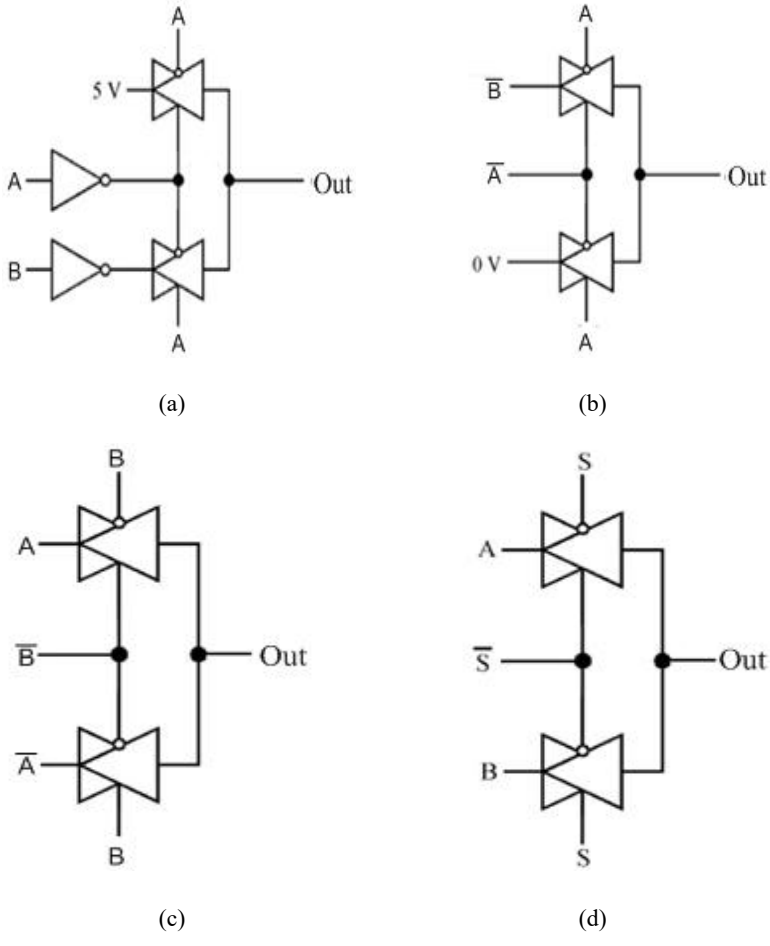


3 Logic style

The performance of logic families varies with logic styles. Again, logic styles' performance depends on technologies. To observe the effect of CMOS and CNTFET technology on the well-known basic gates and circuits, CMOS, CPL and transmission gate (TG) logic styles are chosen.

Figure 2 shows CNTFET-based static CMOS (C-CMOS) logic to realise the basic logic gates such as NAND, NOR, MUX and XOR. Whereas, Figure 3 and Figure 4 show the CNTFET-based complementary pass-transistor (C-CPL) and CNTFET-based transmission gate (C-TG) to realise the same basic gates, i.e., NAND, NOR, MUX and XOR, respectively.

Figure 4 (a) TGL-based NAND gate, (b) TGL-based NOR gate, (c) TGL-based MUX and (d) TGL-based XOR



4 Design constraints

4.1 Parameters

All the circuits are simulated using Synopsys HSPICE simulator with 90 nm and 32 nm CMOS PDK technologies together with a compact SPICE model for 32 nm CNFET technology. This standard 32 nm CNTFET model (Stanford University, https://nano.stanford.edu/stanford-cnfet-model/) has been considered as MOSFET-like CNFET device. Here, flexibility is given to the designer to choose a transistor with one or more CNTs. Some of the important parameters of the CNFET model such as, Lch (physical channel length), Kgate (the dielectric constant of the high-k top gate dielectric material), Tox (the thickness of the high-k to gate dielectric material), Csub (the coupling capacitance between the channel region and the substrate) and their values considered are 32 nm, 16, 4 nm and 20 pF/m, respectively (Chau et al., 2005).

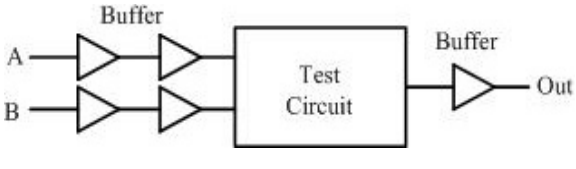
Simulations of all the circuits have been done at a temperature of 25°C. The delay and power dissipated in each circuit are calculated. The PDP is calculated to determine the overall performance of the circuits. PDP is nothing but the multiplication of the average power consumed by the circuits and the maximum delay between inputs and outputs.

All the circuits are simulated with 90 nm and 32 nm CMOS PDK technologies together with 32 nm CNFET model. This standard 32 nm CNTFET model has been considered as MOSFET-like CNFET device. Here, flexibility is given to the designer to choose a transistor with one or more CNTs. Some of the important design parameters of CNTFET are Lch (physical channel length), the mean free path in the intrinsic CNT channel, the length of the doped CNT source-side extension region, the dielectric constant of the high-k top gate dielectric material and the thickness of the high-k top gate dielectric material; their values are 32 nm, 100 nm, 32 nm, 32 nm, 16 and 4 nm, respectively. Other design parameters for CNFET model such as width (by varying the pitch), charity vector (n, m) and the number of nanotubes are individually optimised for each logic style to get least PDP. The number of tubes considered here is 3. The optimised value of pitch and charity is obtained as 2 nm and (19, 0), respectively.

4.2 Test bench

A test bench as shown in Figure 5 has been designed for simulation of outputs in a real environment. All input signals are sent through buffer circuits so that all the inputs that are applied to the circuit appeared at the same time. Simulation has been carried out by varying input supply voltages. The delay is calculated between the inputs and outputs and the worst delay has been recorded. The simultaneously the average power of each of circuits has been observed. Then, the PDP is calculated, which determines the overall performance of the circuit.

Figure 5 Test bench for test circuit



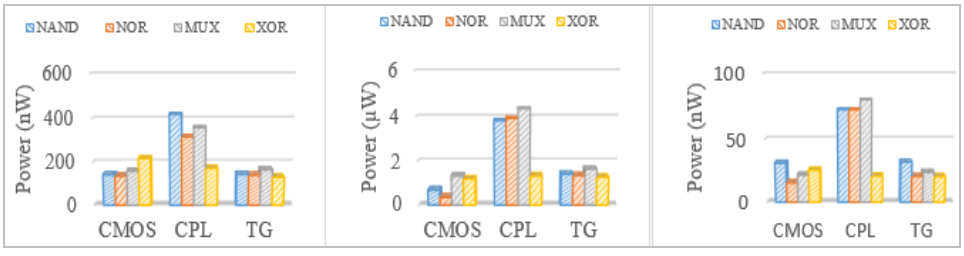
5 Results and discussion

To evaluate the performance of logic gates, two-input NAND, NOR, XOR and MUX are used by taking the conventional CMOS, CPL and TG logic styles with above-mentioned technologies. For the CNFET model, considering the above constraints the simulations are carried out. The supply voltages considered for 90 nm, 32 nm CMOS technologies are 1.2 V and 1.05 V, respectively, whereas for CNTFET model it is 0.9 V. Power, delay and PDPs at a frequency of 200 MHz are calculated and shown in Table 1.

5.1 Total power calculation

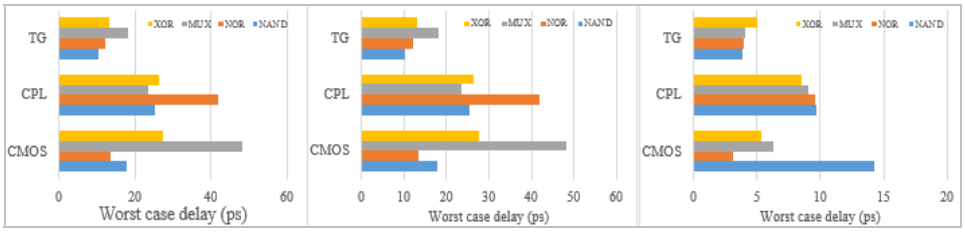
The main components of the power dissipation of a circuit are static power and dynamic power. Static power is the power consumed during any steady-state due to different leakages of MOS transistor. Dynamic power is due to the transitions of signals through the transistor. So, total dynamic power is the summation of power dissipations for all transition and short circuit power dissipation. Capacitor plays a very important role in power dissipation. In the proposed circuit, the sizing of the transistors is done very carefully. To make a comparison of power consumption on technology nodes and logic styles a graph has been plotted as shown in Figure 6.

Figure 6 Power consumption comparison of the circuits at different logic styles at (a) 90 nm bulk-Si (b) 32 nm bulk-Si and (c) 32 nm CNTFET technology nodes (see online version for colours)



(a) (b) (c)

Figure 7 Delay comparison of the circuits at different logic styles at (a) 90 nm bulk-SI MOSFET (b) 32 nm bulk-SI MOSFET and (c) 32 nm CNTFET technology nodes (see online version for colours)



(a) (b) (c)

Table 1 Simulation results for NAND, NOR, MUX and XOR gate

Test circuit	*Logic styles*	*90 nm CMOS technology*			*32 nm CMOS technology*			*32 nm CNTFET technology*		
		Power (μW)	*Delay (ps)*	*PDP (10^{-17} J)*	*Power (nW)*	*Delay (ps)*	*PDP (10^{-18} J)*	*Power (nW)*	*Delay (ps)*	*PDP (10^{-19} J)*
2I/P NAND	CMOS	0.693	17.8	1.2354	142.2	10.9	1.549	31.2	14.3	4.462
	CPL	3.820	25.3	9.664	418	15.6	6.521	72.5	9.73	7.051
	TG	1.42	10.3	1.463	144	7.63	1.098	31.9	3.81	1.212
2I/P NOR	CMOS	0.357	13.4	0.478	136.5	9.45	1.289	15.5	3.11	0.482
	CPL	3.920	41.9	16.425	317	16.46	5.218	72.4	9.62	6.965
	TG	1.36	12.2	1.659	141	7.56	1.066	20.6	3.93	0.809
2I/P MUX	CMOS	1.340	48.1	6.445	159	30.4	4.834	21.7	6.27	1.361
	CPL	4.340	23.4	10.156	358	15.7	5.621	79.9	9	7.191
	TG	1.65	18.2	3.003	166	10.8	1.793	23.9	4.05	0.968
2I/P XOR	CMOS	1.200	27.5	3.3	218	13.9	3.906	25.6	5.36	1.372
	CPL	1.340	26.4	3.534	173	12	2.076	20.9	8.5	1.777
	TG	1.29	13.1	1.69	132	7.85	1.036	20.5	4.97	1.019

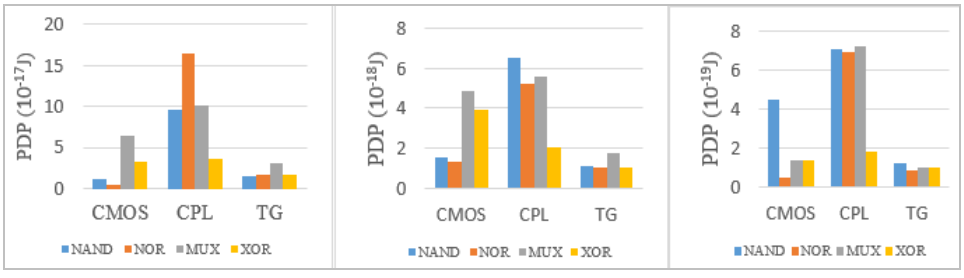
5.2 Delay calculation

The delay is calculated from the time required to get 50% of an input voltage level to 50% of the output voltage level (Hussain and Chaudhury, 2019). The simulated result presented in this work is the worst case delay observed. The delay comparison graph has been shown in Figure 7.

5.3 PDP calculation

Power and delay are inversely proportional to each other, so power and delay alone cannot evaluate the overall performance of a system (Chandrakasan et al., 2003). Hence, PDP that is total energy consumption is evaluated by multiplying power and worst case delay. The PDP comparison graph has been shown in Figure 8.

Figure 8 PDP comparison of the circuits at different logic styles at (a) 90 nm bulk-SI MOSFET (b) 32 nm bulk-SI MOSFET and (c) 32 nm CNTFET technology nodes (see online version for colours)



(a) (b) (c)

5.4 Effects on CMOS logic

In bulk-Si-CMOS, technology both PMOS and NMOS has different size, mobility and current driving capability, so PMOS and NMOS sizing are done separately. But sizing of the transistor with CNTFET technology is easier and provides optimised power, delay, and improved performance. From the simulation results, it is observed that the performance and robustness of the circuits decrease as technology scales down.

Because of self-restoring mechanism, power dissipation has the least effect on CMOS logic as compared to CPL. From the simulation results, it is also observed that CNFET-based CMOS logic gates such as NAND gate, NOR gate and MUX have the least PDP, then CPL logic styles at all supply voltages, exceptional cases have been observed for XOR gates. But in case of CNTFET technology in the all the logic circuits CMOS wins the race over CPL logic style.

5.5 Effects on CPL logic

CPL is advantageous for certain logic gates, e.g., XOR gates, but other basic digital gates show less performance in 90 nm and 32 nm CMOS technologies. CNFET-based CPL gates better than CMOS gates as former has the highest PDP value. But power

consumption is high in CPL logic and hence it is very much wasteful of energy. Further, the circuit complexity of CPL is more and output levels degrade with the technology. The high switching activity in CPL results in more power dissipation. With the scaling down of technology, CPL degrades its performance in terms of power and speed. So, CPL has the least improvement in PDP with technology being scaled-down and it is all because of the threshold drop that results reduced current drive and so slower operation at the reduced power supply.

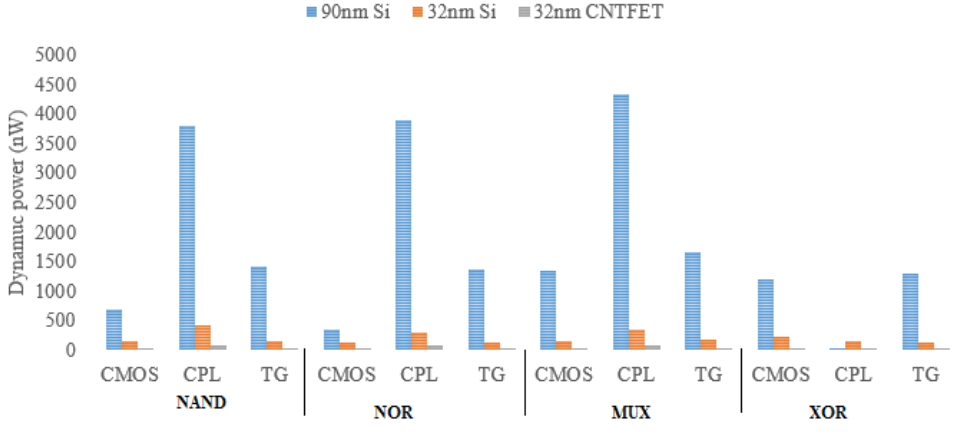
5.6 Effects on TG logic

It is observed that power consumption in the TG is higher than that of CMOS, whether it is lesser than that of CPL logic gates. But the delay is least compared to others. So, the operation of TG logic is faster as compared to CMOS and CPL logic. But overall performance in terms of PDP is higher in some gates whereas it is lower in some other gates.

5.7 Leakage power consumption

The total average power consumed by each of the logic circuits is first obtained through simulation. To make a keen observation, the total average power is examined into two parts as dynamic power and static power. Dynamic power is the power that is dissipated during any transition of the logic (transition mode), whereas static power is the power that is consumed during any steady state of operation, i.e., either in logic 1 or logic 0 (normally, in standby mode). Comparison of dynamic power consumption is shown in Figure 9. Static power is mainly due to the different leakage currents. Hence, it is also known as leakage power consumption. The simulated result of dynamic and static power is shown in Table 2.

Figure 9 Comparison of dynamic power consumption (see online version for colours)



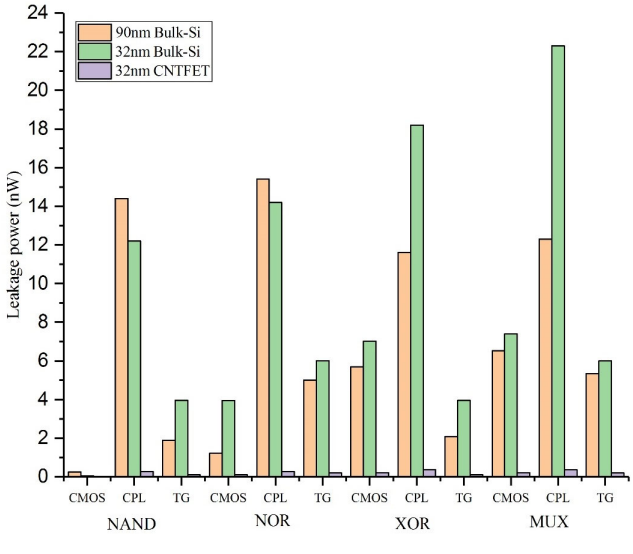
It is seen that for both two input NAND and NOR gates, dynamic power and static power are least in CMOS logic style irrespective of the technology. Exceptional cases have been observed for MUX and XOR circuits. For MUX, though dynamic power is least for CMOS logic in all the three technologies, leakages are least in case of TG logic style. With 90 nm Si technology, the XOR gate has the least dynamic and static power is in

CMOS and TG logic styles respectively. Whereas, with 32 nm Si and 32 nm CNTFET technology, XOR gate has the least dynamic and static power consumption in TG logic style. The worst case for all the technologies is observed in CPL logic. It is all because CPL has more number of transistors. Thus, more the switching activity and hence more the dynamic power. It is also observed that in CPL logic static power dissipation is highest. The main reason behind high static power consumption in CPL logic is due to more leakage currents as a number of transistors are more.

Table 2 Dynamic and static power consumption

Test circuit	*Logic styles*	*90 nm Si technology*		*32 nm Si technology*		*32 nm CNTFET technology*	
		Dynamic power (μW)	*Static power (nW)*	*Dynamic power (nW)*	*Static power (nW)*	*Dynamic power (nW)*	*Static power (pW)*
2I/P NAND	CMOS	0.693	0.256	142.15	0.050	31.1787	21.3
	CPL	3.8056	14.4	405.8	12.2	72.228	272
	TG	1.41812	1.88	140.04	3.96	31.797	103
2I/P NOR	CMOS	0.35578	1.22	132.55	3.95	15.39	110
	CPL	3.9046	15.4	302.8	14.2	72.128	272
	TG	1.355	5	134.99	6.01	20.405	195
2I/P MUX	CMOS	1.3343	5.7	151.99	7.01	21.485	215
	CPL	4.3284	11.6	339.8	18.2	79.528	372
	TG	1.64791	2.09	162.04	3.96	23.792	108
2I/P XOR	CMOS	1.19348	6.52	210.6	7.4	25.383	217
	CPL	1.3277	12.3	150.7	22.3	20.537	363
	TG	1.28465	5.35	126	6	20.303	197

Figure 10 Leakage power comparison of different technologies (see online version for colours)



To illustrate the comparison of leakage power, a bar diagram is shown in Figure 10. It is observed that in the simple logic gates such as NAND and NOR gates, the minimum leakage power is found to be with CMOS logic style. But for complex circuits like MUX and XOR gate, though dynamic power is minimum in CMOS logic style, leakage power is minimum in TG logic style. It is also observed that as CMOS technology is scaled down from 90 nm Si technology to 32 nm bulk-Si technology, leakage power consumption increases sharply. Whereas, with 32 nm CNTFET technology leakage power is much lesser than that of other technologies.

6 Conclusions

It is observed from this work that CMOS logic style performs better than other logic styles in bulk-Si MOS technology. The variation of PDP in CPL logic style with different technologies is much worse than that with other logic styles. With bulk-Si technology, CMOS performs better than other logic styles, though exceptional cases have been observed. But with CNTFET technology, the basic gates such as NAND, XOR and MUX, the TG logic style performs better than CMOS and much better than CPL logic in terms of PDP. At 32 nm CNTFET technology, the least power, delay and PDP are observed as 15.5 nW, 3.11 ps and 0.048 aJ, respectively. CMOS logic style CNFET circuits outperform others in terms of low average power consumption as compared to TG and CPL logic styles except for XOR gate, whereas TG outperforms others in terms of speed. It is also observed that as bulk-Si MOS technology is scaled down, the overall performance of the circuits starts degrading. Leakages do also reverse phenomenon has been observed for CNTFET technology and so CNFET technology is best suited to high-performance systems and for the deep sub-micron technology. Since leakage or static power is also less in CNTFET technology, thus it could be concluded that CNTFET technology is going to suppress other technology in the near future for sub-micron regime circuit design. The logic families considered here are only static types. It is because the static logics are widely used, so dynamic, adiabatic or reversible logics are not considered. This could be a future scope of the work

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