FPGA implementation and analysis of model predictive current control for three-phase voltage source inverter

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Abstract: A detailed investigation of the model predictive current control (MPCC) for a three-phase voltage source inverter (VSI) with an output RL filter is examined in this manuscript. The investigation on VSI and its operating conditions such as dynamic, steady state, transient state condition with balanced and unbalanced loads are explained. The parameter variations such as sampling time, filter inductance and DC-link voltage variations are also explained in terms of load current Total Harmonic Distortion (THD) and inverter switching frequency. During each sampling period, the discrete mathematical model of the system is used to predict the load current for all the inverter switching state. These predictions are estimated using cost function, and so, the switching state which gives minimum cost function is selected and applied to the inverter. The effectiveness of the control technique is verified in MATLAB software and also in real-time hardware setup using Xilinx XCS500E Spartan 3E FPGA board. The detailed simulation and hardware results are included to investigate the implementation.

Keywords: cost function; model predictive current control; sampling time ($T_S$); THD; VSI.

1 Introduction

Current control approach plays an important role in power converters. A variety of current control methods have been utilised to control three-phase inverter. In past few decades, the predictive current control method of power converters has gained more attention, and many researchers showed their interest making it as a hot topic among researchers. Holtz (1994), Kazmierkowski and Malesani (1998) and Rodriguez et al. (2004) provide the detailed information about various linear and nonlinear current control techniques and its applications. The predictive control of power converters had been presented since the 1980s for the control of three-phase voltage source inverter (VSI).
This predictive control is easy to implement, and also it can be applied to a variety of systems with an easy inclusion of constraints. With the advancements in the technology, the predictive control technique is well matched for the control of power converters, and it can be applied successfully to a broad range of applications.

The model predictive current control (MPCC) technique uses a mathematical model of the system for the prediction of load current using all possible switching state of the inverter. Then, the predicted load current and their references are used to evaluate a cost function at the end of each sampling time. Finally, the switching state that is produced at the minimum cost function is selected and applied in the next sampling instant so that an appropriate control action is being selected. This control technique has attracted real-time applications due to its features such as flexibility, inherent decoupling behaviour, fast dynamic, steady and transient response and does not require any modulators when compare with classical controllers. By using hysteresis current controller, it causes resonance problems and which is additionally to increase the size and cost of the filter. And it is not prefer in low power applications due to high switching losses. The linear current control technique needs controller with modulation stage to generate gating pulses to the inverter which requires complex modelling and higher computational capacity (Cortes et al., 2012; Rodriguez et al., 2013; Kouro et al., 2009).

Due to the simplest nature and easiest prediction, the MPCC has been applied to various types of power converters and its applications. The predictive current control with a steady state is analysed for a three-phase VSI (Rodriguez et al., 2007). This concept has been extended to four-leg inverter operation under balanced, unbalanced and nonlinear loading conditions with simulation and hardware (Yaramasu et al., 2013; Rivera et al., 2013), and these control techniques are also implemented on NPC converters (Vargas et al., 2007; Yaramasu et al., 2014), cascaded H-bridge inverters (Cortes et al., 2010), matrix converters (Vargas et al., 2008; Correa et al., 2009), uninterruptible power supplies (Cortes et al., 2009), flux and torque control of an induction machine (Correa et al., 2007; Abad et al., 2008), power control of active front-end rectifiers (Larrinaga et al., 2007; Cortes et al., 2008; Preindl and Bolognani, 2013) and active power filters (Acuna et al., 2014).

However, the detailed investigation on a filter, load and parameter variations for three-phase VSI is not yet described in the literature. So in this manuscript, the MPCC technique has been analysed with various conditions such as dynamic, steady state, transient state, $T_s$ variation, DC-link voltage ($V_{dc}$) variation and filter inductance variation. This paper is organised as follows. Section 2 presents MPCC strategy for three-phase VSI is given in detail. In Section 3, simulation results are presented. In Section 4, Experimental results are presented. Finally, in Section 5, conclusion are drawn.

2 Model predictive current control of power converter

2.1 Three-phase voltage inverter topology

The representation of three-phase VSI with an output filter is shown in Figure 1. This topology has been selected for its clear analysis of a MPCC with an output filter and R-load. The inverter terminal voltages and the corresponding inverter switching states ($S_{in}$) are shown in Table 1.
Table 1  Inverter switching states and voltage vectors

<table>
<thead>
<tr>
<th>Switching states ($S_{sw}$)</th>
<th>$S_a$</th>
<th>$S_b$</th>
<th>$S_c$</th>
<th>Voltage vector ($v j \frac{2}{3} V_{dc}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(S_{sw}) - 1$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$v_0$</td>
</tr>
<tr>
<td>$(S_{sw}) - 2$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>$v_1$ $-(1/3)V_{dc} - j \left(\sqrt{3}/3\right)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 3$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>$v_2$ $-(1/3)V_{dc} + j \left(\sqrt{3}/3\right)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 4$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>$v_3$ $-(2/3)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 5$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$v_4$ $(2/3)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 6$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$v_5$ $(1/3)V_{dc} - j \left(\sqrt{3}/3\right)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 7$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$v_6$ $(1/3)V_{dc} + j \left(\sqrt{3}/3\right)V_{dc}$</td>
</tr>
<tr>
<td>$(S_{sw}) - 8$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>$v_7$ 0</td>
</tr>
</tbody>
</table>

It is a three-leg two-level inverter consisting of six IGBT switches ($S_1$–$S_6$) and each leg of inverter contains two sets of complementary switches. The switching states of the inverter are determined by the switching pulses $S_a$, $S_b$, and $S_c$ as follows:

$$ S_a = \begin{cases} 1 & \text{if } S_i \text{ on and } S_j \text{ off} \\ 0 & \text{if } S_i \text{ off and } S_j \text{ on} \end{cases} \quad (1) $$

$$ S_b = \begin{cases} 1 & \text{if } S_i \text{ on and } S_j \text{ off} \\ 0 & \text{if } S_i \text{ off and } S_j \text{ on} \end{cases} \quad (2) $$

$$ S_c = \begin{cases} 1 & \text{if } S_i \text{ on and } S_j \text{ off} \\ 0 & \text{if } S_i \text{ off and } S_j \text{ on} \end{cases} \quad (3) $$
The vectorial representation of switching pulses can be stated as:

\[ (S_{sw}) = \frac{2}{3}(S_a + aS_b + a^2S_c) \]  \quad (4)

where \( a = e^{-j2\pi/3} \).

The applied output voltage to the filter and load through the inverter are well defined by:

\[ v = \frac{2}{3}(V_{an} + aV_{bn} + a^2V_{cn}) \]  \quad (5)

where \( V_{an} \), \( V_{bn} \), and \( V_{cn} \) are the inverter phase to neutral voltages. Then the inverter output load voltage vector \( v_i \) can be related to the switching state \( (S_{sw}) \) and input voltage \( V_{dc} \) by

\[ v_i = V_{dc}(S_{sw}) \]  \quad (6)

\[ v_i = V_{dc}\frac{2}{3}(S_a + aS_b + a^2S_c) \]  \quad (7)

By evaluating each of inverter switching states in (7), total eight number voltage vectors \( (v_0 - v_7) \) can be created. In that \( v_0 \) and \( v_7 \) attain the same value as zero-voltage vector, and so total seven dissimilar vectors are delivered by three-phase VSI, as it can be seen in Figure 2.

**Figure 2** Voltage vectors generated by the inverter (see online version for colours)

In balanced load condition, the load current can be expressed as:

\[ i = \frac{2}{3}(i_a + ai_b + a^2i_c) \]  \quad (8)

The vector equation of the load current can be expressed as

\[ v = (R + R) i + L \frac{di}{dt} \]  \quad (9)
where \( R_f, R, L_f \) and \( v \) are the filter leakage resistance, load resistance, filter inductance and voltage generated by the inverter, respectively.

### 2.2 Predictive current control

The MPCC strategy of VSI is presented in Figure 3. It uses the mathematical model of the system, load current and switching state to predict the future load current (Rodriguez et al., 2007).

**Figure 3** Block diagram of MPCC-based VSI (see online version for colours)

The system model derivative \( dx/dt \) from the Euler first-order approximation can be expressed as:

\[
\frac{di}{dt} = \frac{i(k) - i(k-1)}{T_s} \tag{10}
\]

Substituting Eq. (10) in Eq. (9), the following expression as:

\[
v = (R_f + R)i + L_f \frac{i(k) - i(k-1)}{T_s} \tag{11}
\]

Then the inverter load current at instant \( k \) is expressed as:

\[
i(k) = \frac{1}{(R_f + R)T_s + L_f}\left[ L_f i(k-1) + T_s v(k) \right]. \tag{12}
\]

Shifting the load current \( i(k) \) in one-step forward in the future, then the load current can be expressed as:
where $i(k)$ load current and $v(k+1)$ predicted load voltage which is the optimal variable to be calculated.

The major intention of MPCC is to reduce the error between the references and predicted current which is defined as quality function or cost function. To obtain this intention, the inverter switching state which is going to reduce $g$ is chosen and applied at the time of next sampling period.

In the next sampling period, the error between the defined reference current and the predicted load current can be expressed by

$$g = |i_{\text{ref}}(k+1) - i(k+1)|$$

where $i_{\text{ref}}(k+1)$ is the reference current and $i(k+1)$ is the inverter predicted load current. In this paper for computational simplicity, absolute error is used. Other methods can be used to identify the cost functions such as error squared and it is represented as follows:

$$g = (i_{\text{ref}}(k+1) - i(k+1))^2$$

Finally, the minimum cost function is selected, and corresponding switching pulses are given to the inverter.

The MPCC algorithm is implemented in MATLAB embedded function block. The functional block operates in the discrete update technique that is based on sampling time defined for the algorithm. When verifying the MPCC algorithm through MATLAB simulations, the cost function calculation deals with the $(k+1)$ predictions (Rodriguez et al., 2007), whereas in real-time verification, the delay provided by the gate drivers, processor and switching devices is unavoidable. So, $(k+2)$ is used to compensate the delay (Cortes et al., 2012). The MPCC algorithm with delay and without delay compensation is shown in Figures 4 and 5, respectively.

A step-by-step procedure for the execution of MPCC strategy is given below:

- The present instant DC-link voltage and load current are measured.
- In order to compensate the delay, the load current is estimated at instant $(k+1)$ using optimal voltage vector and switching state and supply voltage.
- The load voltage vector at instant $(k+1)$ is estimated by using eight possible switching state and supply voltage.
- The load current at instant $(k+2)$ is predicted using voltage vectors and currents at $(k+1)$ instant.
- Evaluating the cost function by comparing predicted load current with the reference currents.
- During each sampling period, the cost function minimisation is carried out so that the control objective is met.
Finally, the switching state that gives minimum cost function is selected and applied to the inverter.

3 Simulation results

The operation of MPCC-based three-phase VSI under various operating conditions is simulated in MATLAB/Simulink software by using Simpower System toolbox with the parameters as indicated in Table 2. To investigate the performance, seven different cases have been selected for simulation such as dynamic response, steady state, transient state, the variation of $T_s$, variation of $V_{dc}$ and variation of filter inductance. The reference current is defined manually. The detailed concept of prediction, cost function and switching states are discussed earlier. The six different cases, from dynamic state to $V_{dc}$ variations, are carefully chosen to determine the effectiveness of the control method.

Table 2 Inverter and load parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>DC-link voltage</td>
<td>100 V</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Sampling time</td>
<td>100 $\mu$s</td>
</tr>
<tr>
<td>$R$</td>
<td>Load resistance</td>
<td>$R_{a, b, c} = 10 \Omega$, $R_a = 10 \Omega$, $R_b = 5 \Omega$, $R_c = 15 \Omega$</td>
</tr>
<tr>
<td>$R_f$</td>
<td>Filter leakage resistance</td>
<td>0.05 $\Omega$</td>
</tr>
<tr>
<td>$L_f$</td>
<td>Filter inductance</td>
<td>12 mH</td>
</tr>
</tbody>
</table>
3.1 Dynamic response

In case 1, the dynamic response of the system is tested under two scenarios, such as balanced load and unbalanced load. Here, the value of the reference current ($i_\alpha$) is decreased from 4 to 2 A, whereas the value of reference current ($i_\beta$) is static with the help of it in which the decoupling nature of the current control loop is found.

The simulation results for dynamic performance of the reference current and load current are given in Figure 6a and b, respectively. From the results, the controller has an excellent dynamic response and load current that closely follows reference, and its dynamic response is fast and the coupling effects between $i_\alpha$ and $i_\beta$ are absent.

**Figure 6** Dynamic response of reference and load current: (a) balanced load and (b) unbalanced load (see online version for colours)

3.2 Steady-state response

The performance of MPCC in steady-state condition is investigated in the case of 2. The following two main scenarios are assessed to track the behaviour of the controller during the steady-state condition.

Scenario 1 shows the steady-state response of balanced reference and balanced load, and scenario 2 shows the steady-state response of balanced reference and unbalanced load.

Figure 7a and b illustrates the performance of MPCC with two scenarios: the actual load current and followed with the reference current with less ripple content. This exhibits a good tracking characteristics of the current references. The THD of the load
current for the two types of loads is found to be 4.52 and 4.25%, respectively. Switching frequency \((F_{SW})\) for the two types of loads is found to be 2.395 and 1.952 kHz, respectively.

**Figure 7** Steady-state response of reference and load current: (a) balanced load and (b) unbalanced load (see online version for colours)

\[\text{Figure 7} \quad \text{Steady-state response of reference and load current: (a) balanced load and (b) unbalanced load (see online version for colours)}\]

3.3 **Transient state response**

The performance of MPCC in transient state condition is considered under two cases: in the first case, the reference current changes from 4A to 2A and 2A to 4A with balanced load, and in the second case, a step change in reference current from 4A to 2A and 2A to 4A with unbalanced load, respectively, as shown in Figure 8a and b. The load current follows the reference immediately without any overshoot.
3.4 Sampling time variations

The plots for the THD versus filter inductance and $F_{SW}$ versus filter inductance for different values of $T_s$ are shown in Figure 9a and b, respectively. In this case, the $T_s$ of the controller varies from 5 to 200 µs. At that time period, the THD of the load current and $F_{SW}$ of the inverter are changed with $T_s$ variations. For a filter inductance greater than 12 mH, for all $T_s$, the value of THD is minimum. At instance, when $T_s$ is 5 µs, the THD of the load current is only 1.95% for 10 mH filter values, whereas for the same inductance when $T_s$ is 200 µs, the THD value is 10.5%.

When increasing the $T_s$ greater than 5 µs for the same filter inductance value, the THD is gradually increasing, and so, it reaches the maximum value. Similarly, the inverter $F_{SW}$ decreases for the increase in the value of the filter inductance from 12 to 30 mH for all $T_s$ values. The THD of the load current has an important relation to the inverter $F_{SW}$, and the THD is high when $F_{SW}$ is low. When increasing the filter inductance, the THD decreases, and vice versa.
inductance and $T_S$ greater than 30 mH and 200 ms, respectively, the load current will not be in sinusoidal nature. Hence, the load current THD is maximum. In Figure 9a and 9b, one can remark that the load current THD is lesser and inverter $F_{SW}$ is greater for larger filter inductance at minimum $T_S$ and vice versa.

**Figure 9** Simulation results of (a) %THD and (b) FSW with filter parameter and TS variations (see online version for colours)

3.5 **Filter parameter variations**

In this case, the filter parameter variations are analysed under two scenarios.

Scenario 1: By varying the inverter filter inductance value and by giving the information to the controller (FIC).

Scenario 2: By varying the inverter filter inductance value and the information is not given to the controller (FINC).

By investigating the THD and $F_{SW}$ of both scenarios according to the given filter inductance, it can be finalised that whenever the filter inductance is low (5 mH), there exists a large variation of THD and $F_{SW}$ compared with other values of inductance, which is shown in Figure 10a and 10b. Even the filter parameter change does not have more impact on the behaviour of the MPCC strategy. The load current is effectively to track their references.
3.6 Perturbations in DC-link voltage

In this condition, the variation of $V_{dc}$ is analysed with MPCC control technique. Here, the $V_{dc}$ value is changed from 60 to 160 V with balanced reference and balanced load to examine the THD and $F_{SW}$ behaviour. By investigating, the THD and $F_{SW}$ according to the given $V_{dc}$ value are shown in Figure 11a and b.
In the inverter, $V_{dc}$ is fixed as a 60 V and the THD of the load current and $F_{SW}$ of inverter are greater than 6% and 0.5 kHz, respectively, whereas the inverter $V_{dc}$ is increased to 80 V and load current THD was decreased to less than 4% and $F_{SW}$ was greater than 1 kHz, respectively, and while the $V_{dc}$ is set as a 100, 120 and 140 V, the THD and $F_{SW}$ are increased. From this, it can be obtained that for lesser than 60 V, the THD is high and $F_{SW}$ is minimum whereas for greater than 100 V, the THD and $F_{SW}$ are increased gradually, the load current THD is less than 5%, and desirable $F_{SW}$ is noticed from 80 to 120 V. Even though the DC-link voltage varies, the load current is to track their reference effectively.
4 Hardware implementation

An experimental setup for the MPCC-based three-phase VSI is developed in the research laboratory to validate few simulation results as shown in Figure 10. The Xilinx Spartan-3E field programmable gate array (FPGA) controller is used to handle the control process. The intelligent power module (IPM) is used as a model of three-phase VSI. The actual load current is measured using a current transformer, and $V_{dc}$ is measured using LEM voltage transducer. The FPGA is purely digital in nature, so the sensed feedback voltage and current signals are given to the analogue to digital converters (ADCs) of FPGA board. The reference current is defined manually, and the reference and actual load current are compared to determine the minimum cost function, and the corresponding cost function switching states are given as a gate pulse to VSI.

For hardware testing the resistive load with 10 ohms and filter inductance with 12 mH, frequency of 50 Hz is used. The complete predictive control algorithm is executed by the FPGA controller at every 100 μs. By varying autotransformer, the input of the IPM is set to maintain the VSI $V_{dc}$ as 100 V. VHDL is used to create the algorithm, and it is tested and synthesised by using Xilinx ISE 10.1 platform for a preliminary validation of the control scheme. The simulated waveform for reference current using Model Sim is shown in Figure 13b. The snapshot of the tested and compiled VHDL code is shown in Figure 13a. Once the code is synthesised, the bit file for the program is created and configured on the XILINX/SPARTAN-3E FPGA target device. The program is embedded on FPGA kit, and it behaves as an FPGA controller, which depends on MPCC. The switching pulse is delivered by the processor, which has the ability to drive the VSI along with gate driver circuits and protection circuits as shown in Figure 14.

Figure 13 (a) MPCC program, (b) model sim output of reference current and (c) photograph of patran3E FPGA (see online version for colours)
By implementing MPCC algorithm in digital signal processors (DSP), it consumes large computation power due to the operation of the high sampling frequency. But MPCC algorithm can be implemented in the Xilinx FPGA, in which it satisfies all the requirements such as it consumes less power for high sampling-frequency operation, fast prototyping, simple designing of software and hardware, high-speed computation, flexibility and parallel processing operation. An FPGA contains hundreds and millions of gates, which can be programmed according to our requirements. The FPGA is capable of processing the instruction in parallel and 16 channel can be read simultaneously, which helps implement high-speed algorithms.

The measurement is noted from a four-channel USB mixed signal oscilloscope (Agilent-MSO6014A) and Two-channel digital signal oscilloscope (Agilent-DSO-X 2002A). The parameters of the converter and control system are given in Table 2. The four cases have been experimentally verified. The detailed waveforms of reference currents, load currents and $V_{dc}$ of four cases are shown in Figures 15–19 with balanced and unbalanced loads using VSI prototype.
Figure 15  Experimental results concerning dynamic response of reference current, load current and $V_{dc}$ with (a 1,2,3) balanced load and (b) unbalanced load (see online version for colours)
Figure 16 Experimental results concerning steady-state response of reference current, load current and $V_{dc}$ with (a1,2) balanced load, (b1,2) unbalanced load (see online version for colours)
Figure 17 Experimental results concerning transient response of reference current, load current and $V_{dc}$ with (a1,2,) balanced load and (b1,2) unbalanced load (see online version for colours)
Figure 18  Experimental results concerning (a) reference current and load current, (b) tracking behaviour with TS of 100 µs (see online version for colours)

Figure 19  Experimental results concerning (a) reference current and load current (b) tracking behaviour with TS of 50 µs (see online version for colours)
The dynamic response of the system is tested with two scenarios such as balanced load and unbalanced load. The results for dynamic performance are given in Figures 15a, 15b, and 15c. These results are similar to the simulation results. It is seen that the reference and load currents closely follow each other, and it has an excellent dynamic response. The coupling effects between $\alpha$ and $\beta$ are absent.

Figure 16a and 16b illustrate the performance of MPCC under steady-state condition with balanced and unbalanced loads. In balance load condition, the actual load current is to track their references with small ripple content. The THD of the load current for the two type of loads is found to be 10.17 and 9.86 %, respectively. And switching frequency ($F_{SW}$) for the two type of loads is found to be 2.190 and 1.841 kHz, respectively. The reference and load values are same as discussed in simulation section. This result also proves that the MPCC performs better under steady-state operating conditions with a balanced and unbalanced load.

Figure 17a and b illustrate the performance of MPCC under transient state condition with a balanced and unbalanced load. It can be clearly seen from here that the actual current tracks the reference current precisely, and the waveforms are smooth without any overshoots and undershoots during the transient period. The effectiveness of MPCC in sampling time variations is shown in Figures 18 and 19.

The FPGA controller is first set to the $T_S$ of 100 µs. The reference current is set to 2A, and load current is produced as per given reference input. The green line is the reference current, and the yellow line is the load current. With the $T_S$ of 100 µs, the FPGA controller is switched at an $F_{SW}$ of 1.805 kHz. The output contains slight ripple content, due to the lower $F_{SW}$. The THD for this condition is 11.20% as shown in Figure 18a and b. Then the FPGA controller is set to the $T_S$ of 50 µs as shown in Figure 19a and b. With a $T_S$ of 50 µs, the $F_{SW}$ is 3.172 kHz, and the THD for this condition is reduced to 9.44%, due to the increasing $F_{SW}$. The summary of simulation and experimental results is presented in Table 3. The gate triggering pulses from the FPGA controller for the inverter switches ($S_1$, $S_3$) are captured using the DSO as shown in Figure 20.

**Figure 20** Experimental results concerning Gate triggering pulses (see online version for colours)
Table 3 Summary of simulation and experimental results

<table>
<thead>
<tr>
<th>Case</th>
<th>Simulation (k+1)</th>
<th>Experimental (k+2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>%THD</td>
<td>$F_{sw}$ (kHz)</td>
</tr>
<tr>
<td>Steady-state analysis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(IRef = 4 A, TS = 100 µs)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Balanced reference balanced load</td>
<td>4.52</td>
<td>2.39</td>
</tr>
<tr>
<td>Balanced reference unbalanced load</td>
<td>4.25</td>
<td>1.95</td>
</tr>
<tr>
<td>Sampling time variation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(IRef = 2 A, balanced load)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 µs</td>
<td>7.06</td>
<td>1.91</td>
</tr>
<tr>
<td>50 µs</td>
<td>4.39</td>
<td>3.27</td>
</tr>
</tbody>
</table>

5 Conclusion

In this manuscript, a MPCC-based three-phase VSI is designed and analysed with Matlab software and also with Xilinx Spartan-3E FPGA controller-based prototype. The experimental results shows that the control strategy gives a better performances and close relation to the simulated results. The better steady-state response and fast dynamic and transient state response with balanced and unbalanced load have been achieved. In addition, the control algorithm has been examined with sampling time, filter inductance and DC-link voltage variations. The results show that the control method can compensate for perturbations in filter and load parameter changes though the load currents continue to effectively track their references. Furthermore, the MPCC is more suitable and easily extended to other power electronic converters with different applications because it is simple design and does not require any modulating stages.

References


