Systematic design strategy for DPL-based ternary logic circuit

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Abstract: This work proposes novel strategy to design 2-input ternary (base-3) logic circuits using double pass-transistor logic (DPL). The concept has been explored with respect to 2-input TXOR gate. The circuit diagram of proposed DPL-based TXOR, TAND and TOR logic gate is presented. The proposed T-Cells are designed and optimised using BSIM3 device model with 1.8 V supply rail and at 25°C temperature on TSMC 0.18 µm CMOS technology. The transient response from T-Spice simulation is validated and the speed-power performance is recorded. Next, the 2:9 ternary decoder based on proposed idea has been explained. The decoder circuit is also designed with 1.8 V supply rail at 25°C temperature on TSMC 0.18 µm CMOS technology. The trit value '0', '1' and '2' are represented with 0 V, 0.9 V and 1.8 V respectively. As per simulation result the proposed 2:9 ternary decoder dissipates 383.57 µW average power and takes 64.87 ps to generate final output.

Keywords: double pass-transistor logic; DPL; hot-spot; ternary (base-3) system; wave-pipelining; 2:9 ternary decoder.

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1 Introduction

Present binary-based VLSI circuits/systems especially system-on-chip (SOC) suffers from highly complicated interconnect with large fan-in/fan-out setback. The resultant localised heat (hot-spot) is a major problem for modern high-density digital IC (VLSI chip) and that can be severe with increased operating speed. The hot-spot makes the IC unreliable and increases the rate of IC failure (Saha et al., 2018; Saha and Pal, 2018). Research on multi-valued logic (MVL) (Hurst, 1984) shows that the ternary (base-3) (Alexander, 1964; Yoeli and Rosenfeld, 1965; Wu, 1990; Vudadha et al., 2018; Vudadha and Srinivas, 2018a; Srinivasu and Sridharan, 2017; Ghiye et al., 2014; Vudadha and Srinivas, 2018b; Shahrom and Ali Hosseini, 2018; Sahoo et al., 2017; Kang et al., 2017) has a potential to replace conventional binary (base-2) number system to overcome problems associated with binary-based processing due to faster computation, reduced interconnect complexity, reduced fan-in/fan-out, less storage requirement and so on for modern digital world. Due to aforesaid advantages the ternary logic became centre of attraction among researchers from long back (Alexander, 1964; Yoeli and Rosenfeld, 1965). However, dealing with three-logic levels instead of two (binary) is a major bottleneck for ternary system designer (Vudadha and Srinivas, 2018a; Srinivasu and Sridharan, 2017; Ghiye et al., 2014). Inherent ON/OFF characteristic of practical solid-state devices makes binary implementation feasible (Saha et al., 2018). However, due to growing difficulties with binary-based digital system design and to cope up with current end user demand there is a renewed interest about ternary among researchers and that can be evidenced from Saha and Pal (2018), Vudadha et al. (2018), Vudadha and Srinivas (2018a), Srinivasu and Sridharan (2017), Ghiye et al. (2014), Vudadha and Srinivas (2018b), Shahrom and Ali Hosseini (2018), Sahoo et al. (2017) and Kang et al. (2017).

The wave-pipelining is a technique in architecture level to improve speed-power performance of digital system (Burleson et al., 1998; Saha et al., 2013, 2017). The maximum operating speed depends not on the critical path delay but on the delay dispersion between fastest and slowest path of the wave-pipelined/time-equalised circuit (Burleson et al., 1998). The elimination of intermediate latches/registers makes the system more speed-power-area efficient as compared to conventional register pipelining (Saha et al., 2013). The destructive effect of clock-skew thus can also be minimised with wave-pipelining strategy. The detail discussion about wave-pipelining is out of scope for the present study. Interested readers are directed to (Burleson et al., 1998; Saha et al., 2013, 2017). The double pass-transistor logic (DPL) (Saha et al., 2017; Hang and Zhou, 2011, 2010; Parthasarathy and Sridhar, 1998; Suzuki et al., 1993) offers favourable characteristics for efficient wave-pipelining. Designing DPL-based ternary logic circuit for speed-power efficient wave-pipelining is an open challenge. In this regard Hang and Zhou (2010) presented some basic ternary cells based on DPL. However no systematic

strategy to design DPL-based ternary logic circuit is given in any open literature and is the centre of focus of present work.

In this study the proposed idea to design DPL-based ternary logic circuit from k-map has been explored first in step-wise manner with respect to ternary XOR (T-XOR) circuit. The optimised circuit diagram of T-AND and T-OR gate as per proposed strategy has been presented. The basic T-cells are designed and optimised based on BSIM3 model parameter with 1.8 V supply rail and at 25°C temperature on TSMC 0.18 μm CMOS technology. The 'trit' value '0', '1' and '2' are represented with 0 V, 0.9 V and 1.8 V respectively. The functionality of designed circuit has been tested with T-Spice simulation using W-edit of Tanner EDA V.13. The speed-power performance of designed circuit is recorded. Next, the proposed concept has been applied to construct 2:9-ternary decoder. The circuit structure along with working principle is explained. The complete decoder circuit is designed and optimised on TSMC 0.18 μm CMOS technology with aforesaid operating condition and supply rail. 'Trit' value '0', '1' and '2' are once again represented by 0 V, 0.9 V and 1.8 V respectively. T-Spice simulation satisfied the functionality of proposed circuit. The performance parameters are tabulated.

The rest of the paper is organised as follows: Section 2 explores the design strategy of proposed DPL-based ternary logic circuits and also presents the simulated results of some basic T-cells. The theory, architecture and simulation results of 2:9 ternary decoder based on proposed idea is explained in Section 3. Paper is concluded in Section 4.

2 Proposed design strategy of ternary logic cell and simulated result

This section explains the proposed idea to design DPL-based ternary logic circuit with respect to two-input T-XOR-gate. The k-map for TXOR is presented in Figure 1. Two ternary inputs to the TXOR circuit is represented with 'X' and 'Y' as also in the k-map in Figure 1. Ternary inverter (TI) is an integral part of proposed structure. Ternary deals with three levels of signalling and hence offer three different inverter circuits namely simple ternary inverter (STI), positive ternary inverter (PTI) and negative ternary inverter (NTI). The I/O relation for all three TI circuit is presented in Table 1. Here in Table 1 the input to the TI circuit is denoted by 'X' and the NTI, STI and PTI output for ternary input 'X' is denoted by 'X_0', 'X_1' and 'X_2' respectively. Also the complement of 'X_0' and 'X_2' is denoted by 'X_{0C}' and 'X_{2C}' respectively. The stepwise explanation of proposed technique to construct DPL-based ternary logic circuit with respect to TXOR-gate is given below:

Figure 1 T-XOR gate k-map

X \ Y	0	1	2	
0	0	1	2	Row-1
1	1	2	0	Row-2
2	2	0	1	Row-3
	Col.-1	Col.-2	Col.-3	

Table 1 I/O relation of different TI

X	*NTI*		*STI*	*PTI*	
	X_0	X_{0C}	X_1	X_2	X_{2C}
0	2	0	2	2	0
1	0	2	1	2	0
2	0	2	0	0	2

Step-1 As shown in k-map of TXOR logic function (Figure 1) the row-1 ('X' = '0') output is always same as input 'Y'. A NMOS device with control variable X_0 (NTI of 'X') and pass variable 'Y' will select row-1 of Figure 1 and will also eliminate the row-2 and 3 from consideration. However, this will not work when 'Y' input is '2' due to inherent pass characteristic of practical NMOS device. To overcome this problem we need to block the col.-3 in Figure 1 first. This can be achieved by the use of another NMOS in series and controlling it by PTI of X (X_2). In order to get output for 'X' = '0' and 'Y' = '2' the PMOS device in parallel with control variable 'X_{0C}' (complement of X_0) will select row-1 of Figure 1. Next to block col.-1 and 2 of Figure 1 a series connected PMOS device with control variable Y_2 (PTI output of Y) can be used. The complete circuit structure for row-1 (X = 0) of Figure 1 is shown in Figure 2.

Step-2 The circuit structure for the intersection of col.-1 ('Y' = '0'), row-2 ('X' = '1') and row-3 ('X' = '2') of Figure 1 can be achieved by two series connected PMOS transistor one with control variable 'X_0' and another with 'Y_{0C}'. The pass-variable here is 'X'. The first PMOS will select 2nd and 3rd row and block 1st row of Figure 1. The second PMOS is responsible to block col.-2 and col.-3 of Figure 1.

Step-3 Consider the case of 'X' = '2', 'Y' = '0' and 'X' = '2', 'Y' = '1'. The NMOS device with pass variable 'Y_0' and control variable 'X_{2C}' will select row-3 of Figure 1. Next to eliminate column-3, a series connected NMOS with 'Y_2' as control variable can be used. Proposed circuit construction for step-2 and step-3 is shown in Figure 3(a) and in Figure 3(b) respectively.

Step-4 This step is responsible to generate circuit structure for 'X' = '2' and 'Y' = '2'. A NMOS device with pass value of ternary '1' and control variable 'X_{2C}' can be used to select row-3 of Figure 1. Following same rule a series connected NMOS device with gate control variable 'Y_{2C}' can be applied to select col.-3. The corresponding circuit structure is presented in Figure 4(a).

Step-5 Next, in this step the corresponding circuit for 'X' = '1' and 'Y' = '2' is generated. First we eliminate row-1 and select row-2 and row-3. This is done by a NMOS device with 'X_{2C}' pass variable and 'X_{0C}' control variable. Next to eliminate 1st and 2nd column, a series connected NMOS with control variable 'Y_{2C}' can be used. The circuit will be inactive for 'X' = '2' and 'Y' = '2' and hence result will be for 'X' = '1' and 'Y' = '2' only. The circuit structure for step-5 is shown in Figure 4(b).

Step-6 This is the final step to design proposed DPL-based ternary logic circuit. The step is responsible to find circuit diagram for 'X' = '1' and 'Y' = '1'. The PMOS with pass input '2' and control variable 'X_{2C}' will select 1st and 2nd row of Figure 1 and eliminate row-3. Next to select 2nd and 3rd row of Figure 1 and eliminate row-1 a series connected PMOS device with 'X_0' gate-control variable can be used. Again column-1 and 2 of Figure 1 can be selected with a series connected PMOS device with 'Y_{2C}' control variable. Finally to eliminate 3rd column another series connected PMOS with 'Y_2' control variable can be used. The circuit construction for step-6 is shown in Figure 4(c).

Figure 2 Step-1 circuit diagram

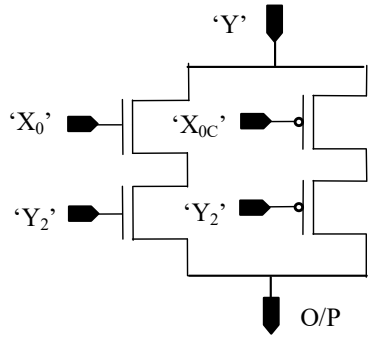
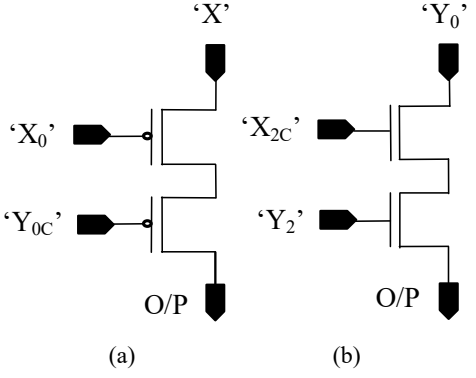


Figure 3 Circuit diagram for, (a) step-2 (b) step-3



The complete circuit diagram for two-input T-XOR gate based on aforesaid strategy is shown in Figure 5. The circuit topology for proposed two-input ternary AND and OR gate is shown in Figure 6. The complementary part is omitted here for the sake of brevity.

In order to validate proposed idea the aforesaid basic ternary cells are designed and optimised based on BSIM3 device model on TSMC 0.18 μm CMOS technology with 1.8 V supply rail and at 25°C temperature using Tanner EDA V.13. Ternary digit value '0', '1' and '2' are represented with 0 V, 0.9 V and 1.8 V respectively. The required NTI, STI and PTI are designed based on idea presented in Hang and Zhou (2010). Designed circuits are tested for all possible input patterns. The custom ternary input to the test circuit has been applied through PWL input source of Tanner EDA. The T-Spice transient

response of designed TXOR, TAND and TOR circuit is presented in Figure 7. Ternary input to the circuit is denoted by 'X' and 'Y' in all the response graph.

Figure 4 Circuit construction for, (a) step-4 (b) step-5 (c) step-6

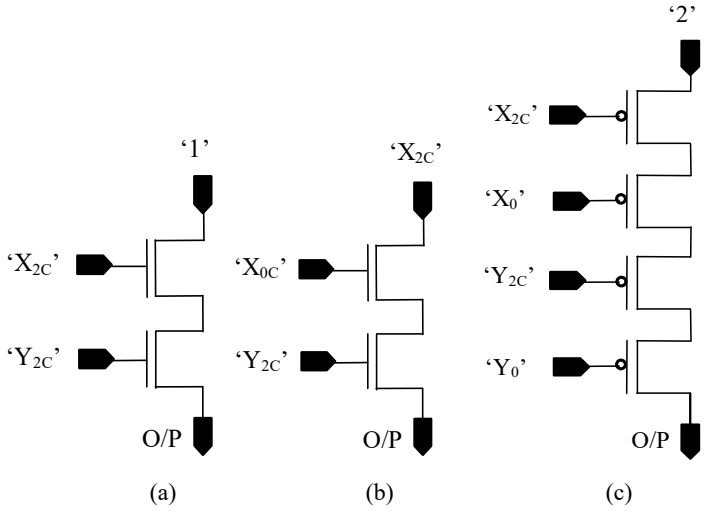


Figure 5 Proposed two-input TXOR circuit

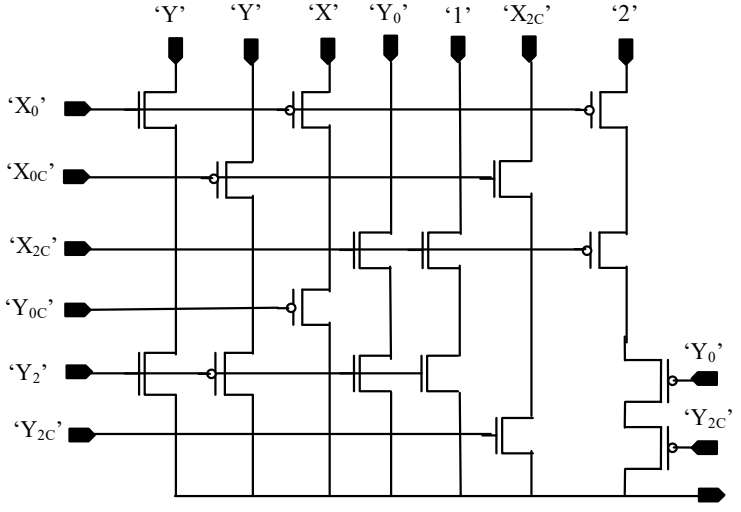


Table 2 Speed-power performance of proposed ternary logic circuits

Design	*Active device count*	*Propagation delay (ps)*	*Power dissipation (μW)*	*Power-delay-product (μW × ps)*
TXOR	40	395.49	145.83	57.67×10^3
TAND	25	173.13	69.17	11.97×10^3
TOR	20	275.74	82.86	22.84×10^3

Figure 6 Proposed two-input, (a) TAND (b) TOR circuit diagram

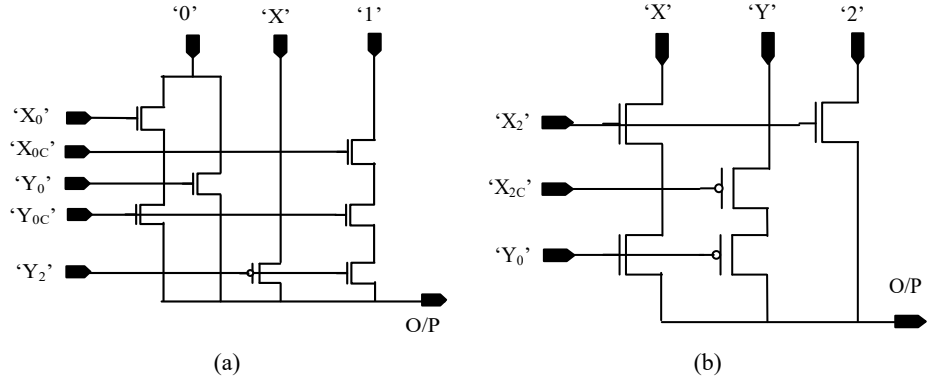
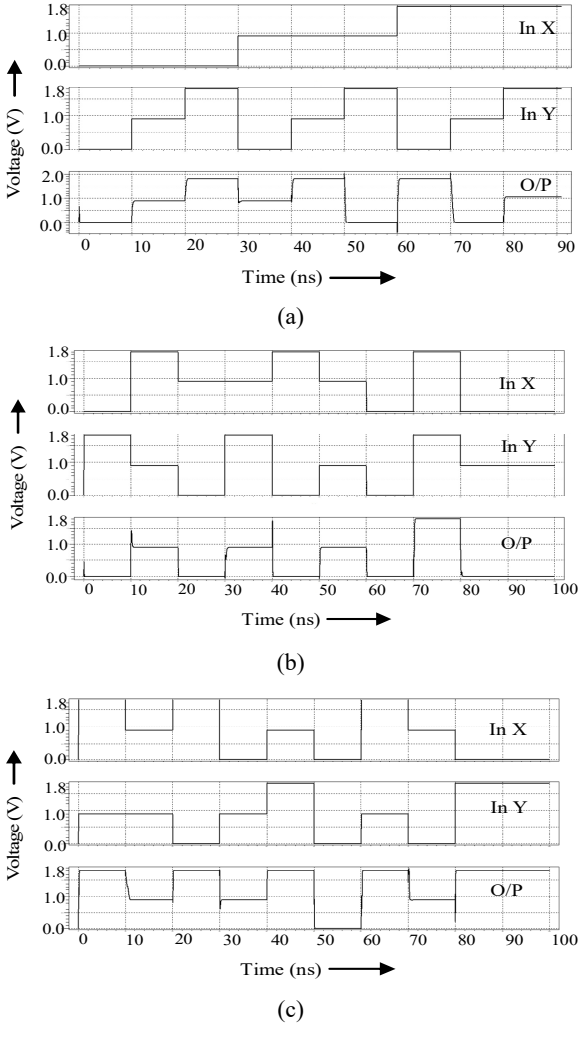


Figure 7 Transient response of proposed, (a) TXOR (b) TAND (c) TOR circuit



The speed-power performance of proposed DPL-based ternary logic cell is tabulated in Table 2. As presented in Table 2, the designed TXOR, TAND and TOR circuit utilises 40, 25 and 20 active MOS devices respectively. The propagation delay for the proposed TXOR, TAND and TOR circuit becomes 395.49 ps, 173.13 ps and 275.74 ps respectively. The designed circuit consumes 145.83 μW, 69.17 μW and 82.86 μW average power for TXOR, TAND and TOR operation respectively. Next, the 2:9-ternary decoder has been designed based on aforesaid strategy. The theory, architecture, working principle and simulated results of proposed decoder is explored in Section 3.

3 Proposed 2:9 ternary decoder: theory and simulated results

The proposed idea has been applied to design 2:9-ternary decoder. Once again the NTI, PTI and STI are the integral part to construct proposed decoder. The I/O relation for TIs are shown in Table 1 and is not repeated in this section. The corresponding NTI, PTI and STI output for ternary input 'X' is denoted by 'X_0', 'X_2' and 'X_1' respectively. The complement of 'X_0' and 'X_2' is represented with 'X_{0C}' and 'X_{2C}' respectively. In order to construct proposed DPL-based circuit structure for 2:9-ternary decoder the truth table is presented first in Table 3. Here in Table 3, the 'X' and 'Y' carries positional weight of 3^1 and 3^0 respectively. The basic block diagram of 2:9 decoder is shown in Figure 8.

Table 3 Truth table of 2:9-ternary decoder

Input		*Output*								
X	*Y*	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8
0	0	2	0	0	0	0	0	0	0	0
0	1	0	2	0	0	0	0	0	0	0
0	2	0	0	2	0	0	0	0	0	0
1	0	0	0	0	2	0	0	0	0	0
1	1	0	0	0	0	2	0	0	0	0
1	2	0	0	0	0	0	2	0	0	0
2	0	0	0	0	0	0	0	2	0	0
2	1	0	0	0	0	0	0	0	2	0
2	2	0	0	0	0	0	0	0	0	2

In order to explain the working principle of 2:9-ternary decoder consider the D_0 output of Figure 8 first. D_0 will have ternary value '2' when input 'XY' = '00'. For other input combinations the D_0 output is '0'. The k-map for D_0 is shown in Figure 9. The proposed circuit for D_0 can be achieved by selecting intersection of row-1 and col.-1 and passing ternary value '2' to the output. Row-1 of Figure 9 can be selected by taking a PMOS device controlling with 'X_{0C}' and passing ternary value '2' through it. Next, col.-1 can be selected by another series connected PMOS with 'Y_{0C}' control variable. Now consider row-2 and row-3 of Figure 9, the corresponding D_0 output is always '0'. The NMOS device with control variable 'X_{0C}' and passing ternary value '0' through it can serve the purpose. Next consider the case corresponding to 'X' = '0', 'Y' = '1' and 'X' = '0', 'Y' = '2' for which D_0 is '0'. A NMOS device with control variable 'X_0' will select entire row-1 of Figure 9. To eliminate col.-1 from consideration the series connected NMOS

with control variable 'Y_{0C}' can be used. The ternary value '0' should be passed through the structure. The complete circuit structure for D_0 is shown in Figure 10. The same strategy has been followed to generate circuit structure for D_1 to D_8 of Figure 8 for the proposed decoder and is presented in Figure 11.

Figure 8 Block diagram of 2:9 decoder

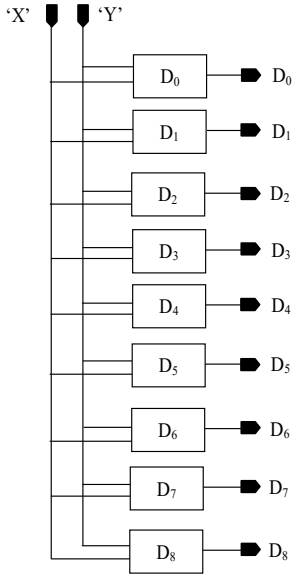


Figure 9 K-map of D_0

X \ Y	0	1	2	
0	2	0	0	Row-1
1	0	0	0	Row-2
2	0	0	0	Row-3
	Col.-1	Col.-2	Col.-3	

Figure 10 The circuit diagram of D_0

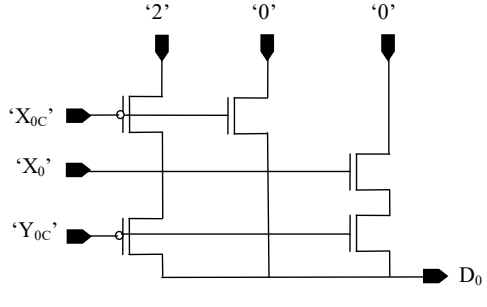


Figure 11 The circuit diagram of, (a) D_1 (b) D_2 (c) D_3 (d) D_4 (e) D_5 (f) D_6 (g) D_7 (h) D_8

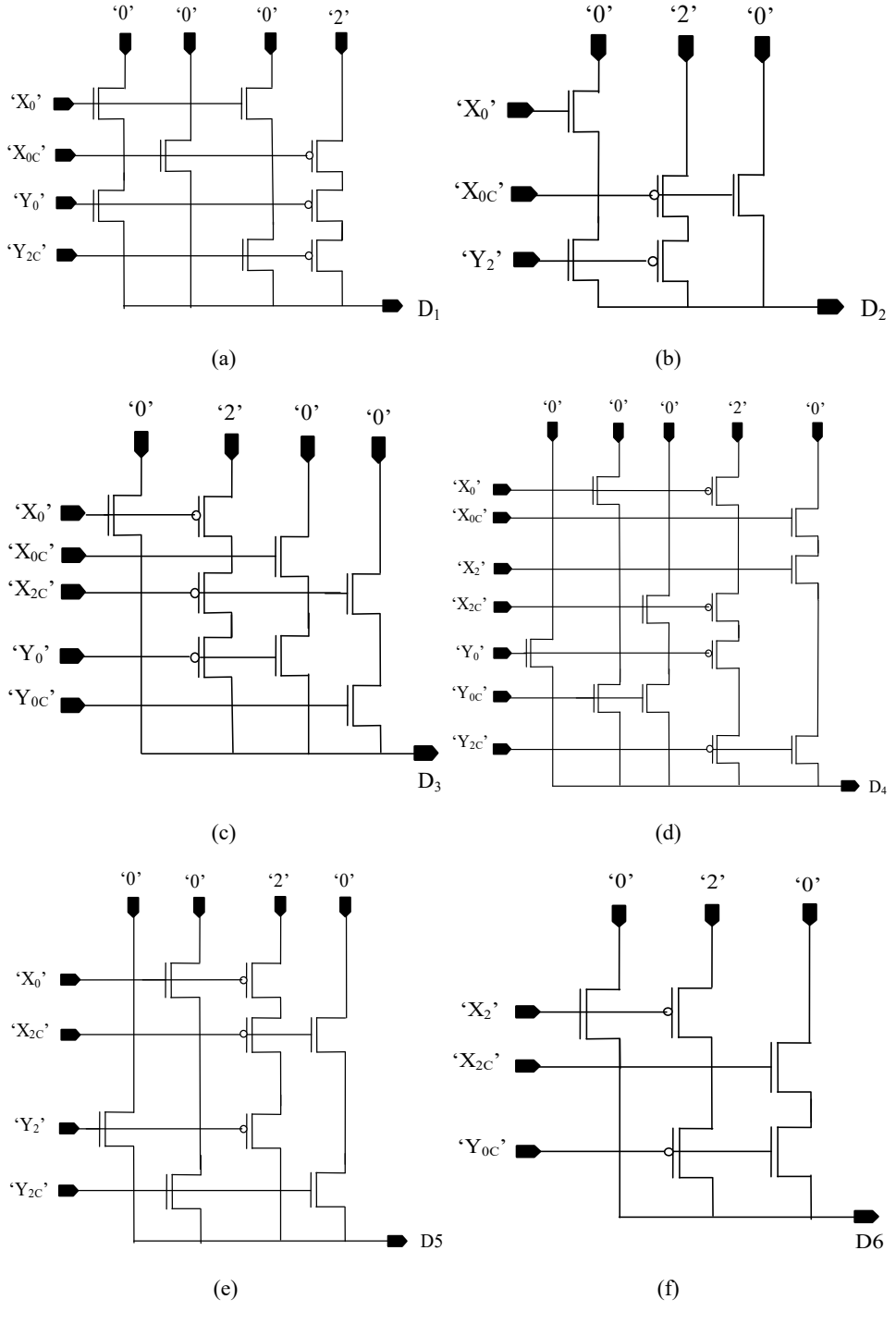
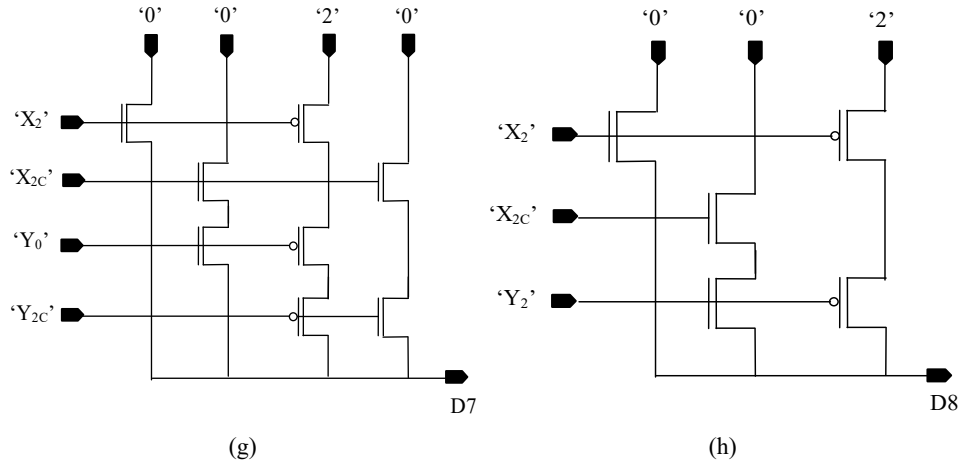


Figure 11 The circuit diagram of, (a) D_1 (b) D_2 (c) D_3 (d) D_4 (e) D_5 (f) D_6 (g) D_7 (h) D_8 (continued)



The complete decoder circuit has been designed on TSMC 0.18 µm CMOS technology using S-Edit of Tanner EDA V.13. The front-end schematic design of the circuit is shown in Figure 12. The circuit optimisation has been done based on BISIM3 MOS model with 1.8 V supply rail and at 25°C temperature. The transient response of designed circuit from T-Spice simulation is presented in Figure 13. The performance parameter of proposed decoder is tabulated in Table 4.

Figure 12 Proposed 2:9 ternary decoder schematic

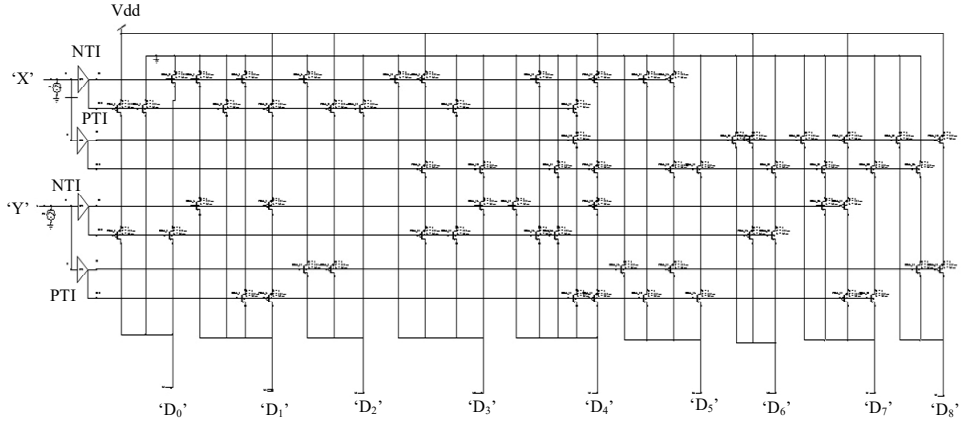
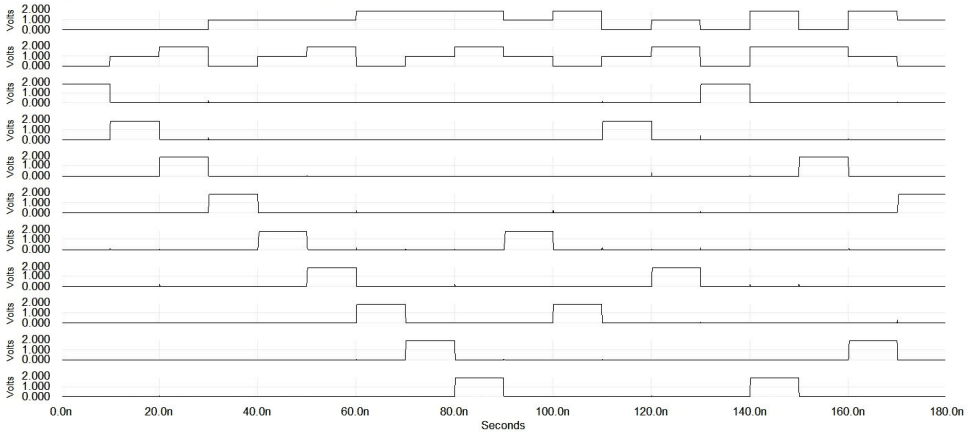


Table 4 Performance of proposed 2:9 ternary decoder

Design	*Active devices*	*Tech.*	*Trit value*	*Avg. power (µW)*	*Prop. delay (ps)*
DPL-based 2:9 ternary decoder	94	TSMC 0.18 µm CMOS	'0' = 0.0 V '1' = 0.9 V '2' = 1.8 V	383.57	64.87

Figure 13 Transient response of decoder



The transient response shown in Figure 13 validates the functionality of designed ternary decoder. The circuit has been tested for all possible input test pattern. 'Trit' value '0', '1' and '2' are denoted by 0 V, 0.9 V and 1.8 V respectively. As per simulation result presented in Table 4, the designed 2:9 ternary decoder circuit needs 94 active MOS devices to construct and dissipates 383.57 µW average power with 64.87 ps propagation delay. As per simulation result the proposed idea can be a good choice to design DPL-based ternary logic circuit for high performance, low-power ternary digital system.

4 Conclusions

In this paper a new systematic strategy to design DPL-based ternary logic circuit is proposed. The proposed technique has been discussed with respect to two input TXOR circuit. Some of basic ternary logic circuits namely TXOR, TAND and TOR are designed and optimised on TSMC 0.18 µm CMOS technology with 1.8 V supply rail and at 25°C temperature. The 'trit' value '0', '1' and '2' are represented with 0 V, 0.9 V and 1.8 V respectively. The designed circuit has been verified for all possible test pattern and the transient response along with speed-power performance is presented. Next, the proposed idea has been applied to design 2:9-ternary decoder. The design strategy with principle of operation is explained. The proposed decoder also has been designed and optimised based on BSIM3 device parameter on TSMC 0.18 µm CMOS technology with 1.8 V supply rail and at 25°C temperature. Once again ternary value '0', '1' and '2' are represented with 0 V, 0.9 V and 1.8 V respectively. Functionality of designed circuit has been tested with T-Spice simulation using W-Edit of Tanner EDA. The custom ternary input to the circuit has been applied with PWL input source of Tanner EDA. The transient response of designed circuit and the speed-power performance is presented. As per simulation, the proposed strategy can be useful to design DPL-based ternary logic circuit for low-power, high-speed ternary digital applications.

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