

International Journal of Power and Energy Conversion

ISSN online: 1757-1162 - ISSN print: 1757-1154

<https://www.inderscience.com/ijpec>

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DOI: [10.1504/IJPEC.2025.10067502](https://doi.org/10.1504/IJPEC.2025.10067502)

Article History:

Received:	15 February 2024
Last revised:	05 April 2024
Accepted:	18 April 2024
Published online:	30 November 2024

Solar PV-fed cascaded multilevel inverters employing zeta converter

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Abstract: The photovoltaic cell produces DC power, while residential, industrial loads and most modern equipment typically require AC power. Thus, there is a need for power converters that can efficiently convert DC to AC. Although two-level inverters are commonly used for this purpose, they suffer from higher total harmonic distortion (THD) and switching stresses. Multilevel inverter (MLI) technology emerges as an effective solution for high-power medium-voltage energy control. This paper examines cascaded multilevel inverters (CMLIs) of varying levels and multiple-carrier sinusoidal switching techniques, conducting a comparative analysis to identify the most suitable switching technique for implementation in solar stand-alone MLIs. Additionally, the study adjusts the duty ratio of the Zeta converter to optimise power extraction from the solar PV system. The primary focus is on the application of CMLIs in stand-alone solar photovoltaic systems, with the study conducted in the Simulink/MATLAB environment.

Keywords: inverter; multilevel inverter; MLI; cascaded multilevel; total harmonic distortion; THD; SPWM; Simulink; solar; photovoltaic; maximum power point tracking; MPPT; perturb and observe; P&O; zeta converter; multiple-carrier SPWM.

Reference to this paper should be made as follows: Naqvi, A.M., Tripathi, P. and Singh, S.P. (2025) 'Solar PV-fed cascaded multilevel inverters employing zeta converter', *Int. J. Power and Energy Conversion*, Vol. 16, No. 1, pp.13–37.

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1 Introduction

A multilevel inverter (MLI), a power electronic device introduced in the 1980s, generates a staircase voltage output by utilising multiple lower-level DC voltages as inputs. In contrast to the commonly used two-level inverter that produces AC voltage from a DC source with two output levels (positive and negative), MLIs offer advantages. The traditional two-level inverter is associated with high switching losses and increased harmonic distortion in the output voltage, leading to the flow of harmonic currents and subsequent losses in the circuit, whereas MLI reduces switching stresses and improves power quality by producing staircase voltage closer to the sinusoidal waveform.

Introduced by Nabae in the 1980s, an MLI synthesises a nearly sinusoidal multilevel voltage output from several DC sources. The stepped waveform it produces offers improved quality and a better harmonic profile, potentially reducing the need for extensive filtering (Rodriguez et al., 2002; Koshti and Rao, 2017; Nabae et al., 1981).

Several MLI topologies have been proposed (Koshti and Rao, 2017; Vijeh et al., 2019). Notable among them are the diode clamped (neutral point clamped – NPC) (Nabae et al., 1981; Rodriguez et al., 2010), flying capacitor (Koshti and Rao, 2017; Rodríguez et al., 2002), and cascaded multilevel inverter (CMLI) (Malinowski et al., 2010; Babaei et al., 2015) which are recognised as classical MLIs. Additionally, there are other topologies such as active NPC (Barbosa et al., 2005; Xu et al., 2019), T-type (Xu et al., 2017), packed U cell (Ounejjar et al., 2011; Vahedi et al., 2018), switched capacitor (Vijeh et al., 2019; Venkataramanaiah et al., 2017; Bikdeli et al., 2021), etc. As MLIs are implemented for a higher number of voltage levels, the number of switches tends to increase. Researchers are actively engaged in the exploration of reduced device count MLIs, aiming to decrease the number of switches and other components (Gupta et al., 2016; Prabakaran and Palanisamy, 2017; Salem et al., 2021a; Vemuganti et al., 2021).

MLIs find extensive applications in various fields, including renewable energy integration (Vahedi et al., 2018; Wu et al., 2020; Xiao et al., 2015), FACT devices (Soto and Green, 2002), power conditioning, drive, and traction applications (Dixon et al., 2010). In renewable energy applications, MLIs can be employed in isolated systems (Madhukar and Sivakumar, 2015; Daher et al., 2008; Sridhar et al., 2015) or grid-connected systems (Amamra et al., 2017; Vosoughi et al., 2020; Vyas et al., 2021).

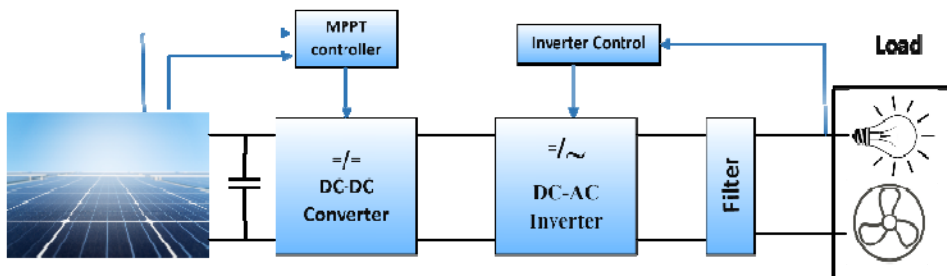
This paper presents CMLI implemented with solar PV-fed zeta converter for three, five, and seven voltage-levels. The zeta converter, characterised by its four-order non-inverting buck-boost configuration and low settling time, is used for the first time in conjunction with a Solar PV-fed CMLI. To determine the most suitable switching techniques (ST) for the solar-PV fed CMLI, various STs are implemented for the CMLI with a constant DC voltage source. These STs are compared based on criteria such as total harmonic distortion (THD) and the ability to achieve equal power extraction.

In this paper, the configuration of a solar-fed CMLI system is elucidated in Section 2. Utilising the perturb and observe (P&O) algorithm, Section 3 details the integration of the zeta converter to extract maximum power from the solar PV cell, followed by feeding the obtained DC power to the load to assess system performance under varying irradiance and temperature conditions. Section 4 delves into the CMLI topology, while Section 5 provides an overview of ST for CMLI. Sections 6 and 7 present the implementation of MLIs with constant DC sources, showcasing different levels and types of ST. Following a comprehensive comparison, the most suitable ST is selected and implemented for the CMLI fed with a solar PV system, as detailed in Section 8. Finally, the paper concludes with a comparison and summary of findings.

2 Configuration of the proposed system

A photovoltaic (PV) cell is a semiconductor device that is capable of converting sunlight into electricity by producing potential differences across its terminal through PV phenomena.

Figure 1 Schematic of a solar PV-connected isolated system (see online version for colours)



The power conversion efficiency of the solar module is only 20%–25% of the solar energy incident in the form of solar irradiation. The maximum power point tracking (MPPT) technique improves the efficiency of the solar panel by extracting maximum power from the solar panel.

MPPT of a PV system has been proposed as a control technique consisting of electronic components to ensure that the maximum possible power will be achieved from

the PV modules under all varying environmental conditions. MPP is achieved by varying and comparing the PV parameters to obtain the value of voltage and current owing to the maximum power. For this purpose, a DC-DC converter is required to vary the operating voltage level and operate it at the value that achieves the maximum possible power at that environmental condition (Subudhi and Pradhan, 2013; Raj and Joshua, 2017; Salem et al., 2021b).

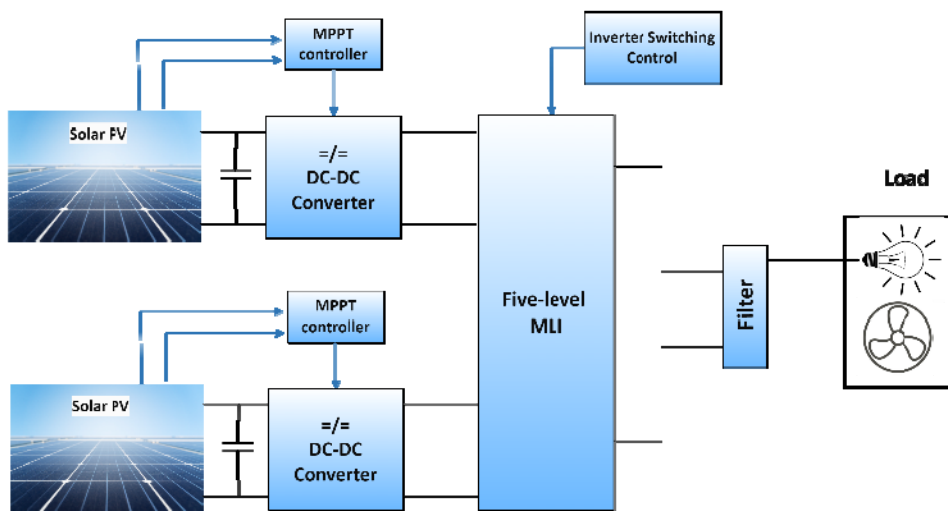
The proper functioning of solar panels is sensitive to being affected by climatic problems so it must be kept under observation (Didi and Azami, 2023).

In a conventional system, two-level inverters are used to convert the DC power to AC, which has its drawbacks like more switching stresses requirement of a large filter, etc. The converted power can be fed to the load.

Figure 2 shows the schematic of CMLI integration with a solar PV system, in which separate solar PV is connected to a DC-DC converter, that works as a separate DC source.

In this paper, CMLIs of different levels are implemented with solar PV. For maximum power extraction from solar PV cells, the P&O algorithm is used to determine the duty ratio of the DC-DC converter, which provides DC input to an H-bridge module of the CMLI as a separate DC source. The switching controller block provides the switching pulses to the switches of the CMLI.

Figure 2 Schematic of solar PV connected MLI (see online version for colours)



3 Maximum power extraction system from solar PV array

The P&O technique is one of the simplest and most popular methods for MPPT. In this method, voltage and power are sensed, and perturbation is adjusted based on the sign of the previous perturbation and the change in power. If power increases, perturbation continues in the same direction; if power decreases, the perturbation direction is reversed. This process continues until oscillation occurs at the maximum power point.

$$\Delta P_n = P_n - P_{n-1} \quad (1)$$

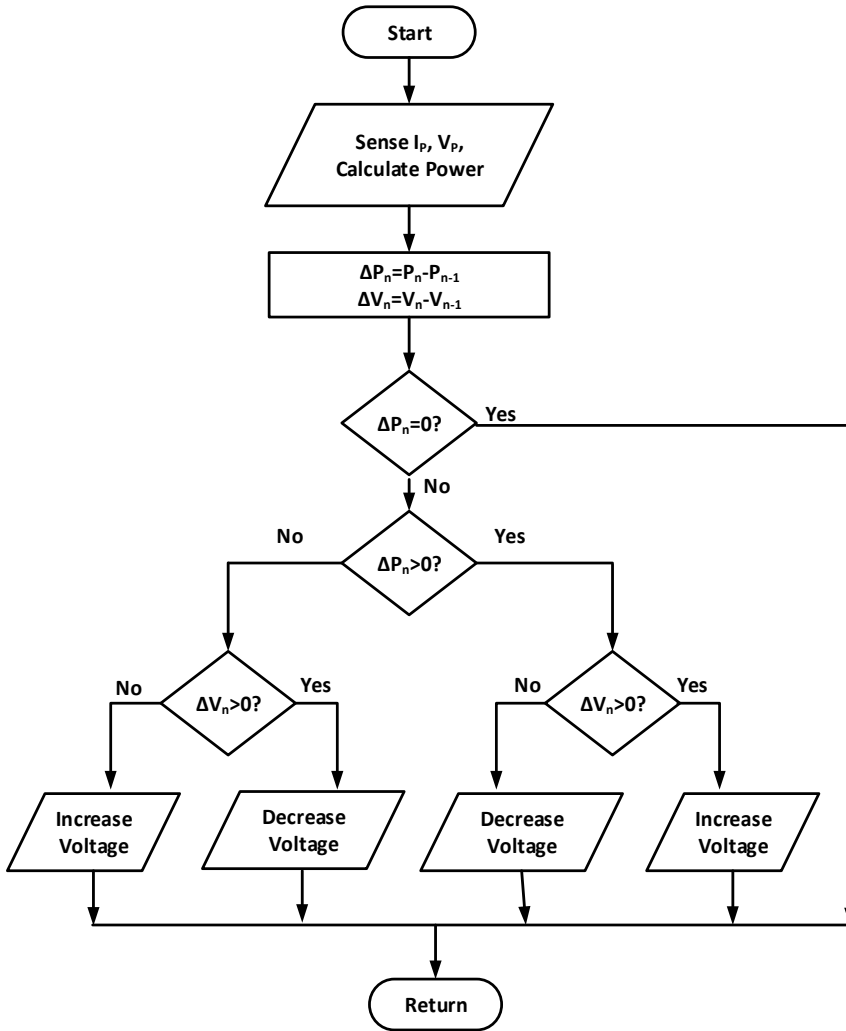
$$\Delta V_n = V_n - V_{n-1} \quad (2)$$

where P_n and V_n is the power and voltage obtained in n^{th} perturbation,

While P_{n-1} and V_{n-1} are the power and voltage obtained in previous $(n - 1)$ perturbation.

Zeta converter, which is unlikely to be a sepic converter, gives non-inverted buck-boost output, is used to make the PV array function around the maximum power point under varying environmental conditions.

Figure 3 Working algorithm of P&O technique



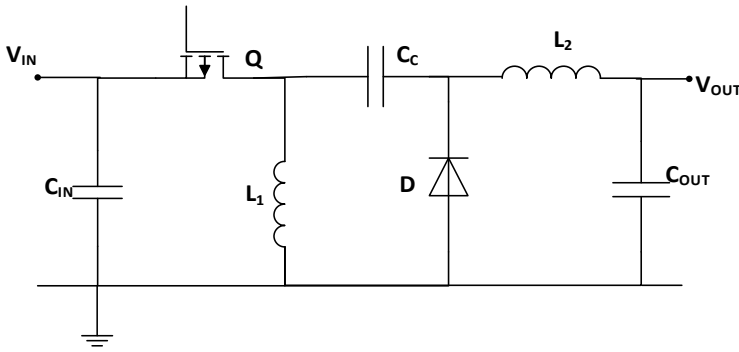
The zeta converter is exclusively designed to operate in the continuous conduction mode, thereby reducing stress on components and minimising output side ripples. This characteristic results in a fairly effective optimisation of the maximum power point. The

advantages of zeta converters are low switching stress, low output ripples, adaptability, and low settling time (Kumar and Singh, 2016; Parthasarathy et al., 2016; Soedibyo and Ashari, 2015).

Table 1 Algorithm of P&O technique

<i>Perturbation</i>	<i>Change in power</i>	<i>Next perturbation</i>
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

Figure 4 Zeta converter



Zeta converter, as shown in Figure 4, consists of a switch Q, a diode D, and four energy-storing devices in which two are inductors L_1 and L_2 , and the other two are capacitors namely CC and COUT.

The working states of the zeta converter consist of two modes, based on the state of the switch.

The on-mode takes place when switch Q is turned on and diode D is in a non-conducting state, while the off-mode follows when switch Q is turned off and diode D is conducting.

With the assumption of 100% efficiency of zeta converter, its duty cycle can be expressed as

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \quad (3)$$

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} \quad (4)$$

MPPT block is used to ensure that the PV array will deliver the maximum power to the load by varying the duty ratio of the zeta converter, which is designed with L_1 and L_2 is 1.0 mH and 1.2 mH, C_1 is 8 μ F while C_2 is 2.25 mF.

Parameters of the Tata Power Solar Systems TP250MBZ at, $T = 25^\circ\text{C}$, $G = 1,000 \text{ W/m}^2$ are as following:

$$I_{mp} = 8.3 \text{ A} \quad V_{mp} = 30 \text{ V} \quad P_{mp} = 249 \text{ W}$$

$$I_{sc} = 8.83 \text{ A} \quad V_{oc} = 36.8 \text{ V}$$

Figure 5 Stand-alone SPV with dc application (see online version for colours)

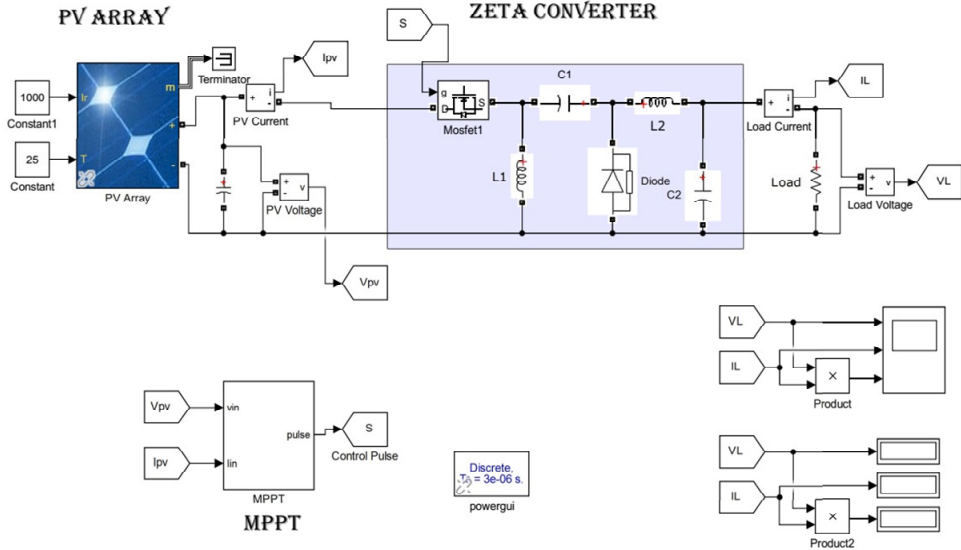
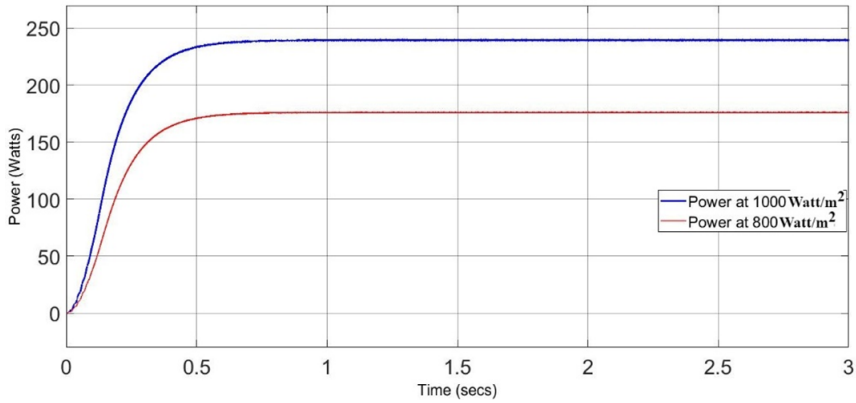


Figure 6 Output characteristic of the array with MPPT at different irradiance and 25° temperature (see online version for colours)

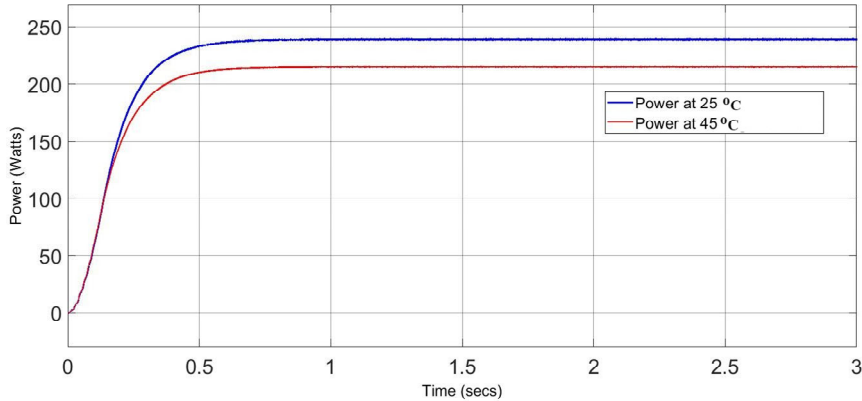


Performance of SPV system with different environmental conditions is observed:

- Output power with different irradiance and temperature of 25°C is shown in Figure 6, as irradiance decreases, the generated voltage of the PV cell also decreases, leading to a reduction in the efficiency of the PV cell.
- Output power with 1,000 W/m² irradiance and different temperatures is shown in Figure 7. As the temperature increases, the current of the PV cell decreases, resulting in a reduction in generated power.

Table 2 Output of MPPT-operated PV array with 100 ohms load in different environmental conditions

	<i>Environmental condition</i>		<i>Voltage (volts)</i>	<i>Current (amp)</i>	<i>Power (watts)</i>
Case 1	1,000 W/m ²	25°C	154.8	1.548	239.7
Case 2	1,000 W/m ²	45°C	146.7	1.467	215.2
Case 3	800 W/m ²	25°C	132.8	1.328	176.3

Figure 7 Output characteristic of the array with MPPT at 1000W/m² irradiance and different temperature (see online version for colours)

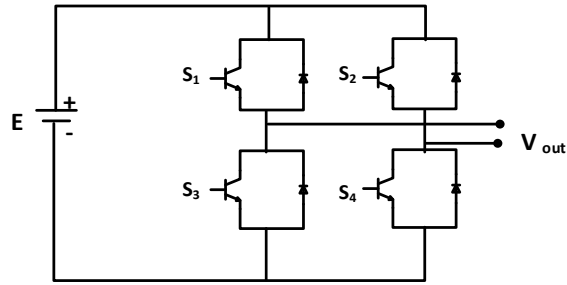
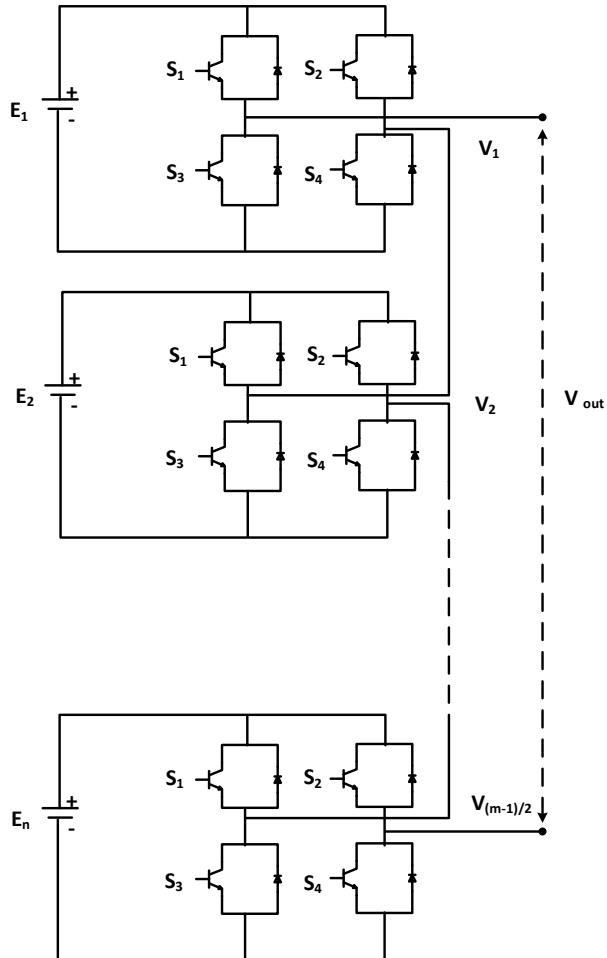
4 Cascaded multilevel inverter

The structure of a CMLI comprises multiple H-bridge modules connected in series on the AC side, generating high-level voltage and achieving high power quality. Each connected H-bridge inverter produces an output of a specific voltage level. The output voltage of the cascaded inverter is the summation of all voltage levels generated by each cell. CMLI can be constructed using identical types, such as a single-phase cascaded H-bridge, or they can be built from different inverter topologies, referred to as hybrid inverters. One notable advantage of this inverter is its requirement of fewer switches compared to diode-clamped MLIs (Koshti and Rao, 2017; Wei et al., 2003).

Each H-bridge inverter is connected to a separate DC source. Each inverter level can produce three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$. In each H-bridge inverter, the dc source is connected to the AC output through different combinations of the four switches, namely S_1 , S_2 , S_3 , and S_4 . When switches S_1 and S_4 are turned ON, $+V_{dc}$ is obtained whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3 . By turning on S_1 and S_2 or S_3 and S_4 , the output voltage is 0.

The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesised voltage waveform is the sum of the inverter outputs.

$$V_{an} = V_1 + V_2 + \dots + \left(\frac{V_{m-1}}{2} - 1 \right) + \frac{V_{m-1}}{2} \quad (6)$$

Figure 8 Basic H-bridge inverter**Figure 9** Generalised CMLI topology

5 Switching techniques

Selecting the appropriate switching strategy is essential for achieving improved output waveforms with minimal THD and low switching losses. Additionally, the choice of modulation control type for an MLI presents a significant challenge. Carrier-based pulse width modulation (PWM) is widely utilised in this domain. High-frequency switching methods involve numerous commutations for the power semiconductors to generate the fundamental output voltage within one cycle (Rodriguez et al., 2002; Koshti and Rao, 2017; McGrath and Holmes, 2002).

5.1 Types of multilevel modulation technique

- Fundamental switching frequency
 - 1 space vector
 - 2 selective harmonic elimination
- High switching frequency
 - 1 multiple carrier sinusoidal PWM
 - 2 space vector PWM

Multiple carrier sinusoidal PWM is further categorised into the following types

- phase disposition (PD)
- phase opposition disposition (POD)
- alternate phase opposition disposition (APOD)
- phase shift (PS) carrier control technique.

5.2 Multiple carrier SPWM

Researchers have introduced several techniques for generating sinusoidal PWM switching signals for inverters, primarily based on two methods: bipolar and unipolar PWM schemes. These methodologies aim to produce AC output with nearly sinusoidal characteristics, including the desired amplitude and frequency. This objective is accomplished through the comparison of a reference sinusoidal control signal, $V_{control}$, operating at frequency f_m , with a carrier waveform, $V_{carrier}$, often triangular in shape, operating at frequency f_c (McGrath and Holmes, 2002; Carrara et al., 1992; Manimala et al., 2011).

For multiple carriers, in which $m - 1$ number of the carriers is required for m level of the inverter, the amplitude modulation ratio m_a is defined as

$$m_a = \frac{V_{control}}{(m-1) \times V_{tri}} \quad (7)$$

$V_{control}$ refers to the maximum amplitude of the sinusoidal reference signal, while V_{tri} denotes the maximum amplitude of the carrier signal.

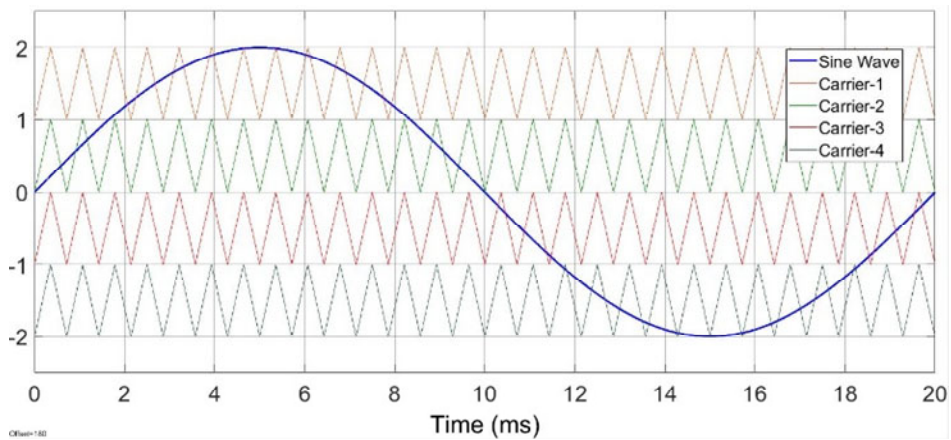
5.2.1 Phase disposition

In the PD technique illustrated in Figure 10(a), a total of $m - 1$ carrier waves is necessary, with m denoting the number of levels of the MLI. All carrier signals maintain phase alignment but are shifted in level. For a five-level MLI, there will be four carrier signals accompanying a reference sinusoidal signal.

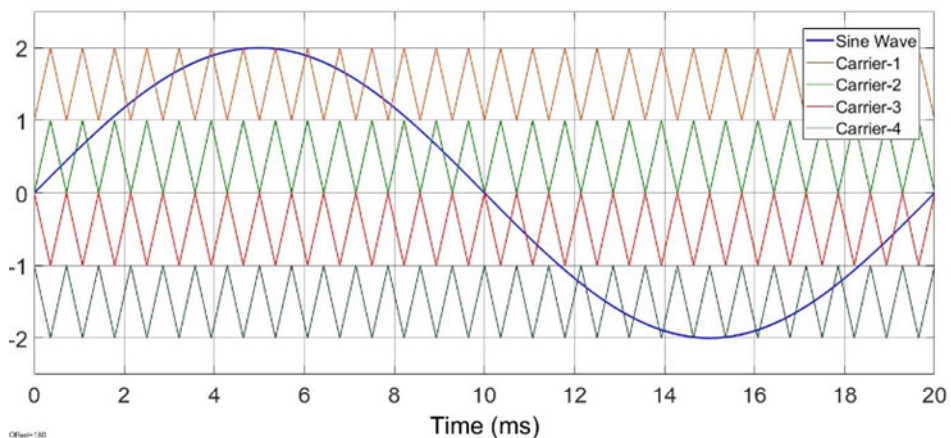
5.2.2 Phase opposition disposition

In the POD technique, shown in Figure 10(b), the carrier signals with positive magnitude are in phase with each other but 180° out of phase with carrier pulses having negative magnitude. For a five-level MLI, there will be four carrier signals above two are in phase with each other but with the lower two pulses they are 180° out of phase.

Figure 10 Multiple-carrier SPWM (a) PD, (b) POD, (c) APOD and, (d) Zoomed-PS technique and (e) PS technique (see online version for colours)

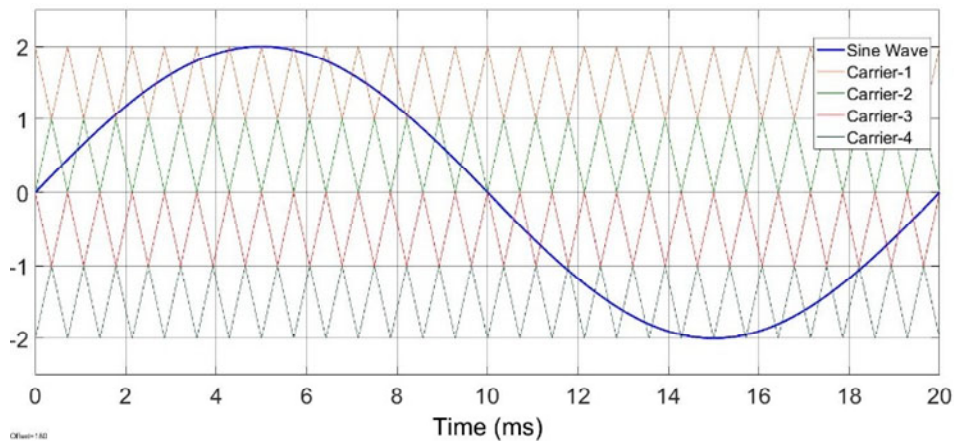


(a)

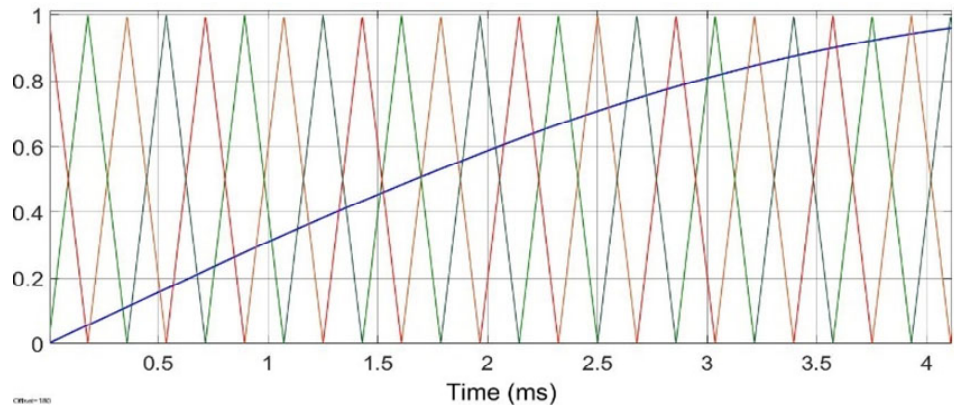


(b)

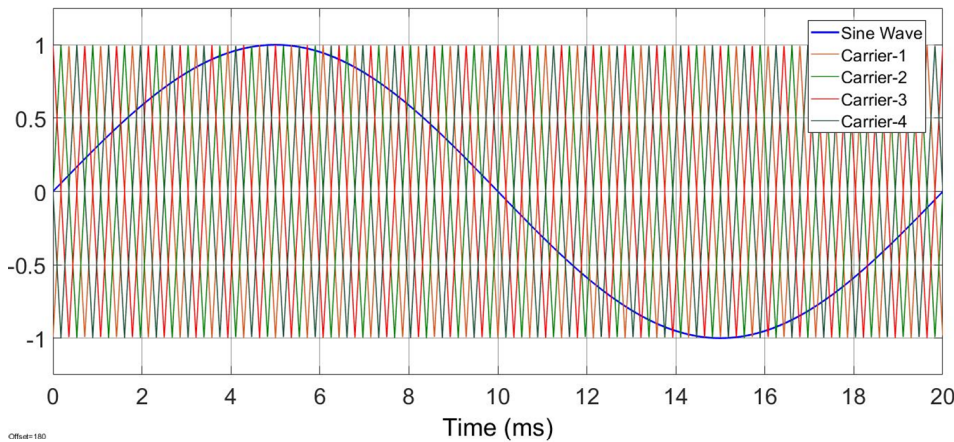
Figure 10 Multiple-carrier SPWM (a) PD, (b) POD, (c) APOD and, (d) Zoomed-PS technique and (e) PS technique (continued) (see online version for colours)



(c)



(d)



(e)

5.2.3 Alternate phase opposition disposition (APOD)

In the APOD technique, depicted in Figure 10(c), all carrier signals are alternately phase-disposed from each other by 180° . For a five-level MLI, this involves utilising four carrier signals with alternating 180° PD.

5.2.4 Phase shift

In the PS technique depicted in Figure 10(d), all carrier waves share the same frequency and amplitude, but each carrier wave is characterised by a distinct PS relative to the others (Rodriguez et al., 2002; Manimala et al., 2011). For best performance, PS should follow the following formula

$$\text{angle shift} = \frac{360^\circ}{m-1} = \frac{360^\circ}{5-1} = 90^\circ \quad (9)$$

6 CMLI with constant DC source

CMLI is implemented with dc sources each of 100 volts and a purely resistive load of 100 ohms. THD spectrum analysis with pure resistive load is shown below, 48.34% THD is present in the 2-level inverter.

THD analysis of a three-level inverter current with pure resistive load is shown below. 41.47% THD is present with a 1.2 modulation index.

Using PS as a modulation technique with a modulation index of 1.2, THD analysis of five-level and seven-level inverter current with pure resistive load gives 21.81% THD and 15.58% THD respectively.

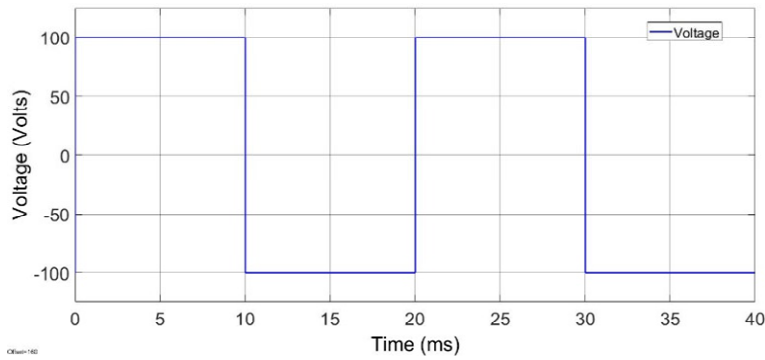
Simulation analysis of different level MLI with load drawing current at unity power factor, i.e. pure resistive load of 100 ohms, shows that with increment level of the inverter, THD level decreases. No change is observed in THD of voltage with the variation of load.

Table 3 THD in inverter current of different level inverters with R load and R-L load

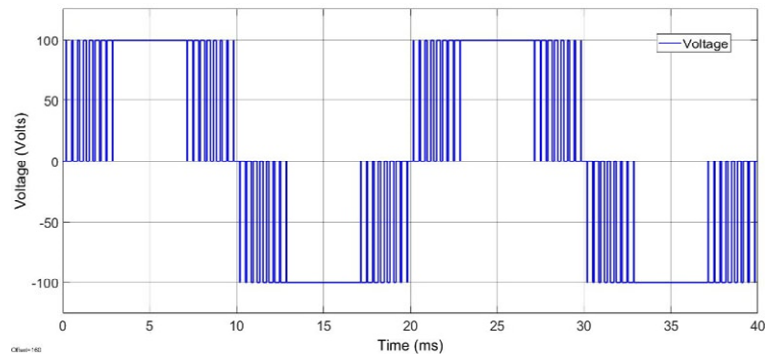
	Power factor	2-level	3-level	5-level	7-level
THD in Voltage (in %)	-	48.34	41.47	21.81	15.58
	Unity	48.34	41.47	21.81	15.58
THD in current (in %)	0.95 lag	28.46	5.52	5.22	5.21
	0.9 lag	23.43	4.52	4.34	4.33
	0.8 lag	18.65	3.59	3.47	3.47

Further, the comparison of THD with an R-L load of 100 ohms and 104.624 mH that draw current at 0.95 power factor lagging, shows the following result. Small inductance smoothens the current waveform and improves the THD in the current. With inductance of 154.7 and 238.16 mH, THD in current further reduces as shown in Table 3.

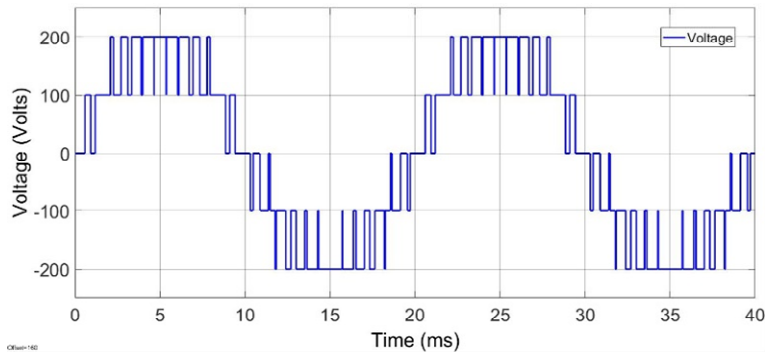
Figure 11 Output voltage of the (a) two-level inverter (b) three-level inverter (c) five-level and (d) seven-level inverter (see online version for colours)



(a)

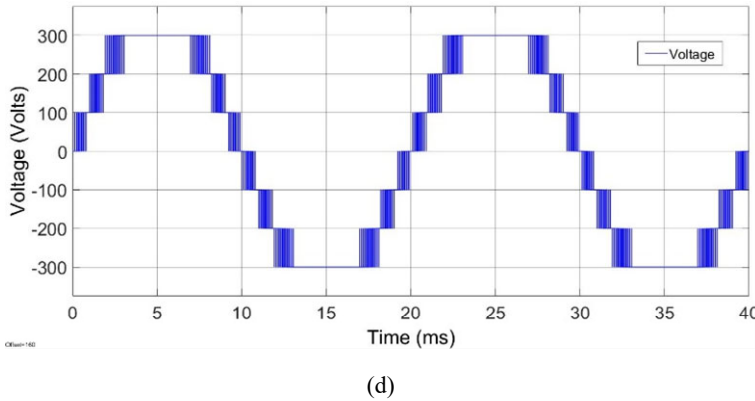


(b)



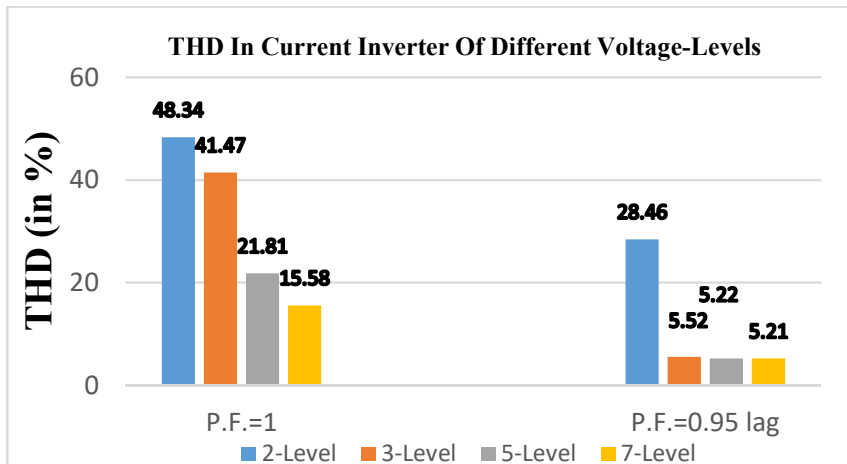
(c)

Figure 11 Output voltage of the (a) two-level inverter (b) three-level inverter (c) five-level and (d) seven-level inverter (continued) (see online version for colours)



Following Figure 12 shows the variation of THD in current with the increment of the level, and also the change in THD with the change in load. THD in current at unity power factor and 0.95 lagging can be observed from Figure 12.

Figure 12 THD in the current of multi-level inverters with different load (see online version for colours)



7 Comparative analysis of different ST

All four MC SPWM techniques possess some different performance features from each other. Simulation analysis of all four types of MC SPWM, i.e., PD, POD, APD, and PS, in a five-level inverter with 1.2 over modulated reference signal and resistive load gives the following THD levels.

All four types of MC SPWM in a seven-level inverter with a 1.2 over modulation index and a resistive load of 100 ohms give the following THD levels.

The difference in the THD in voltage (and also in current as the load is pure resistive) can be observed from the following Figure 13 in which different ST performance with both five-level and seven-level inverter is presented.

Table 4 THD in cascaded five-level and seven-level inverters with different types of switching

		<i>PD</i>	<i>POD</i>	<i>APOD</i>	<i>PS</i>
THD in voltage (in %)	5-level	21.66	21.12	21.89	21.81
	7-level	15.64	14.85	15.41	15.58

Analysis of the power drawn from each DC source in the cascaded multi-level inverter is an important parameter for determining the battery size of the stand-alone system with storage. Each H-bridge inverter extracts power from a separate DC source. This power extraction is dependent on the inverter’s switching behaviour. Therefore, the type of switching implemented influences the power drawn from each particular DC source. For a five-level CMLI, employing PS and PD techniques, the following simulation results are observed.

Figure 13 THD in current cascaded five-level and seven-level inverter with different MC-SPWM (see online version for colours)

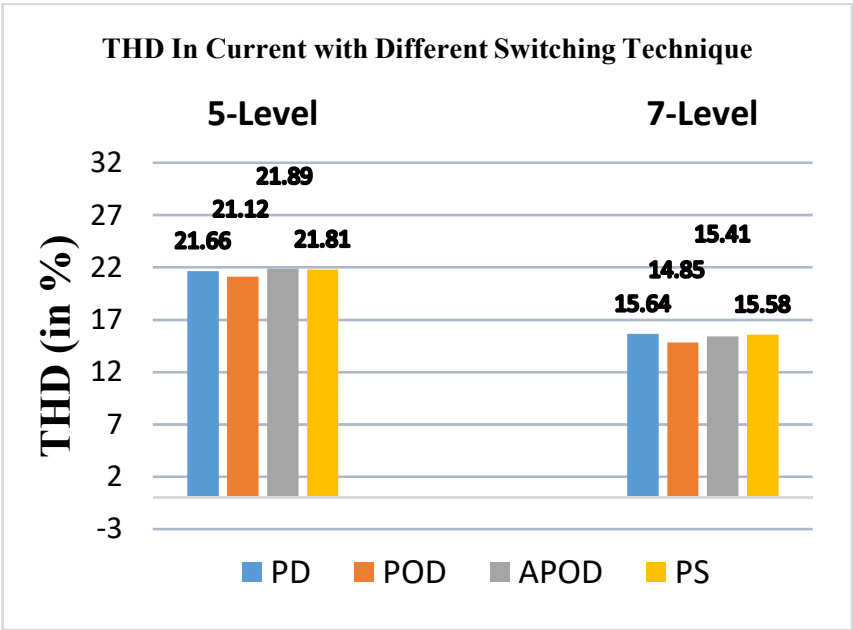


Table 5 Power supplied by two DC sources in a cascaded five-level inverter with different types of SPWM Techniques

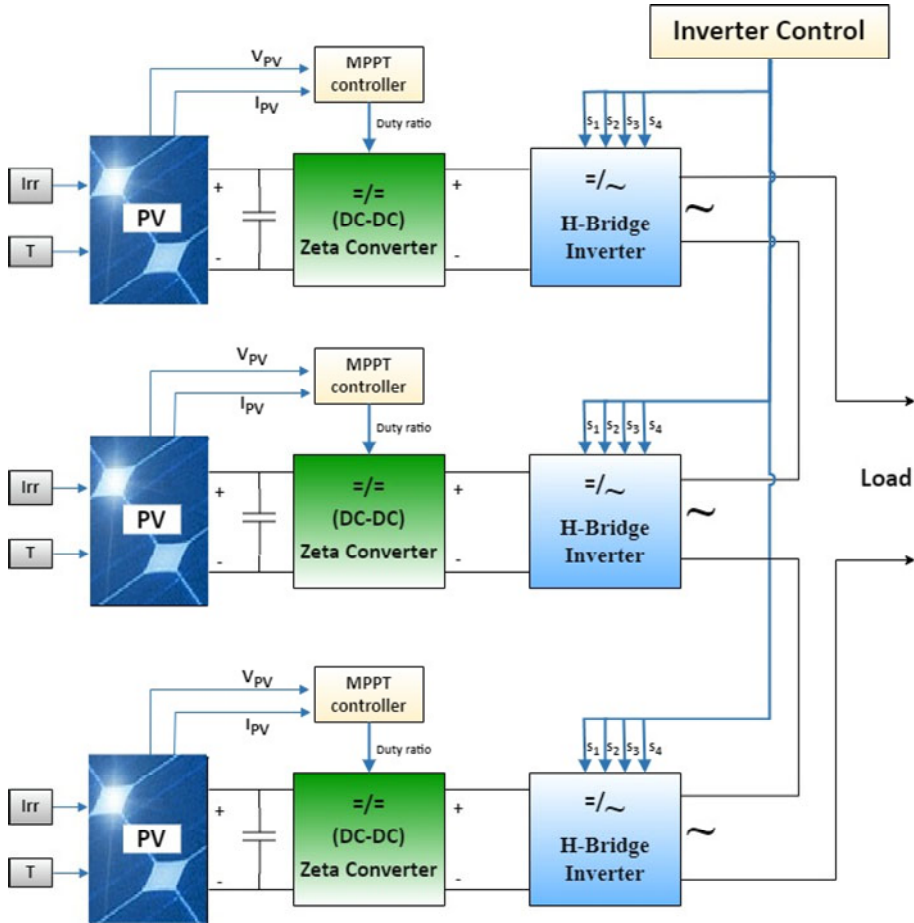
<i>Switching technique</i>		<i>DC Source-1</i>	<i>DC Source-2</i>
Supplied power (in watts)	PD	148.5	120
	PS	135.2	135

Similarly, in the seven-level cascaded multi-level inverter, analysis of power drawn from separate sources gives the following results.

Table 6 Power supplied by three DC sources in a cascaded seven-level inverter with different types of SPWM techniques

	Switching technique	DC source 1	DC source 2	DC source 3
Supplied power (in watts)	PD	225.8	202.1	168.9
	PS	200.3	200.4	200.4

Figure 14 Structure of solar PV-fed seven-level inverter (see online version for colours)



In techniques like PD, POD and APOD switching (level-shifted MC SPWM), unequal power is drawn from separate DC sources. Conversely, in PS switching, equal power is drawn from each source in both five-level and seven-level MLI. For this reason, PS is the preferred ST over the other three MC SPWM methods. In stand-alone Solar PV systems, equal power extraction is favourable for maintaining voltage level symmetry and converter design. Therefore, simple MPPT control will ensure maximum power extraction from each array at the same voltage level.

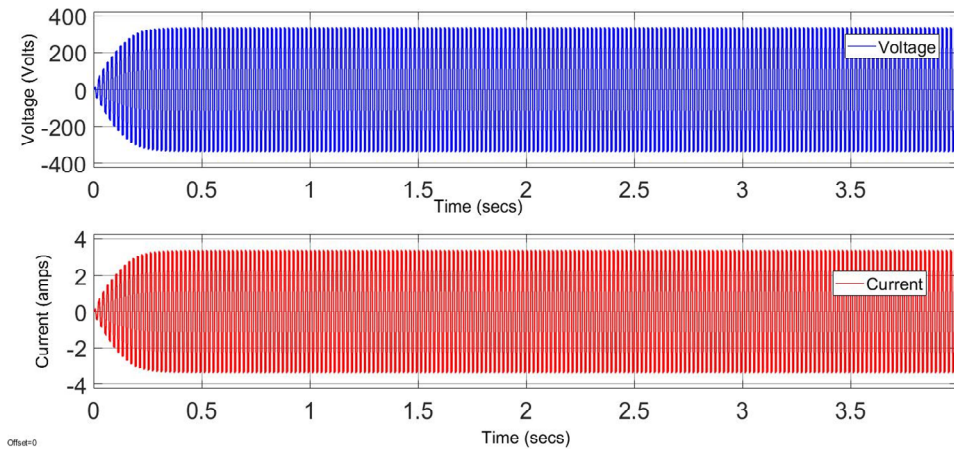
8 Proposed solar PV fed multi-level inverter

In a solar PV-fed MLI, the typical DC source is replaced by a PV array with a well-designed MPPT technique. Each H-bridge cell of the inverter is fed by a separate PV array controlled by an independent MPPT technique.

For both five and seven-level cascaded inverters, the PS modulation technique is employed. Furthermore, a model can be constructed for a five-level cascaded inverter with two cascaded H-bridge inverters, each fed by a separate PV array.

The below illustration depicts a seven-level CMLI, wherein three H-bridge inverters are cascaded and fed by three different PV arrays, each controlled by independent MPPT.

Figure 15 Complete voltage and current waveform of PV array fed seven-level inverter (see online version for colours)



Solar PV array fed MLI of three-level, cascaded five-level, and cascaded seven-level was simulated with two different loads, a purely resistive load of 100 ohms (unity power factor) and an inductive load of 100 ohms and 104.624mH (of 0.95 lagging power factor). A complete simulation of a seven-level inverter for the 4-second period is shown in Fig. 15 after about ten cycles of voltage and current with fundamental frequency can be observed. For analysis purposes of THD stable waveform is considered.

- *Case 1:* Simulation Of PV array fed three-level inverter with (a) R Load (b) R-L Load

THD analysis of current and voltage waveform shows the presence of 41.51% THD with pure resistive load and 5.48% THD with inductive load.

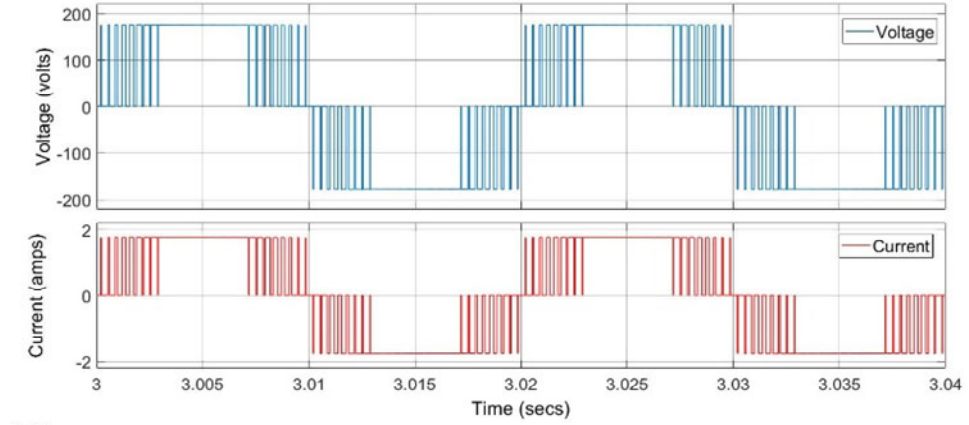
- *Case 2:* Simulation Of PV array fed five-level inverter with (a) R Load (b) R-L load

THD analysis of the current waveform of Cascaded five-level inverter shows the presence of 21.85% THD with pure resistive load and 5.15% THD with inductive load.

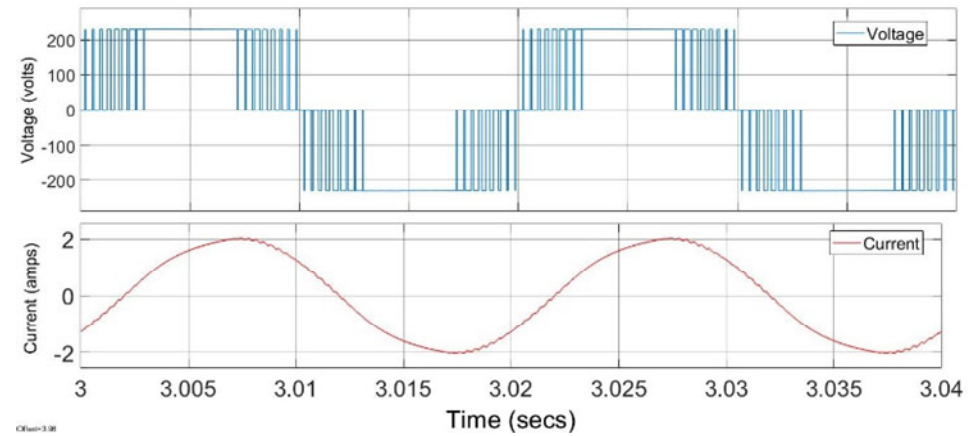
- *Case 3: Simulation Of PV array fed seven-level inverter with (a) R load (b) R-L load.*

THDs analysis of current and voltage waveform shows the presence of 15.63% THDs with pure resistive load and 5.12% THD with inductive load.

Figure 16 Voltage and current waveform of PV array fed three-level inverter with (a) R load (b) R-L load (see online version for colours)

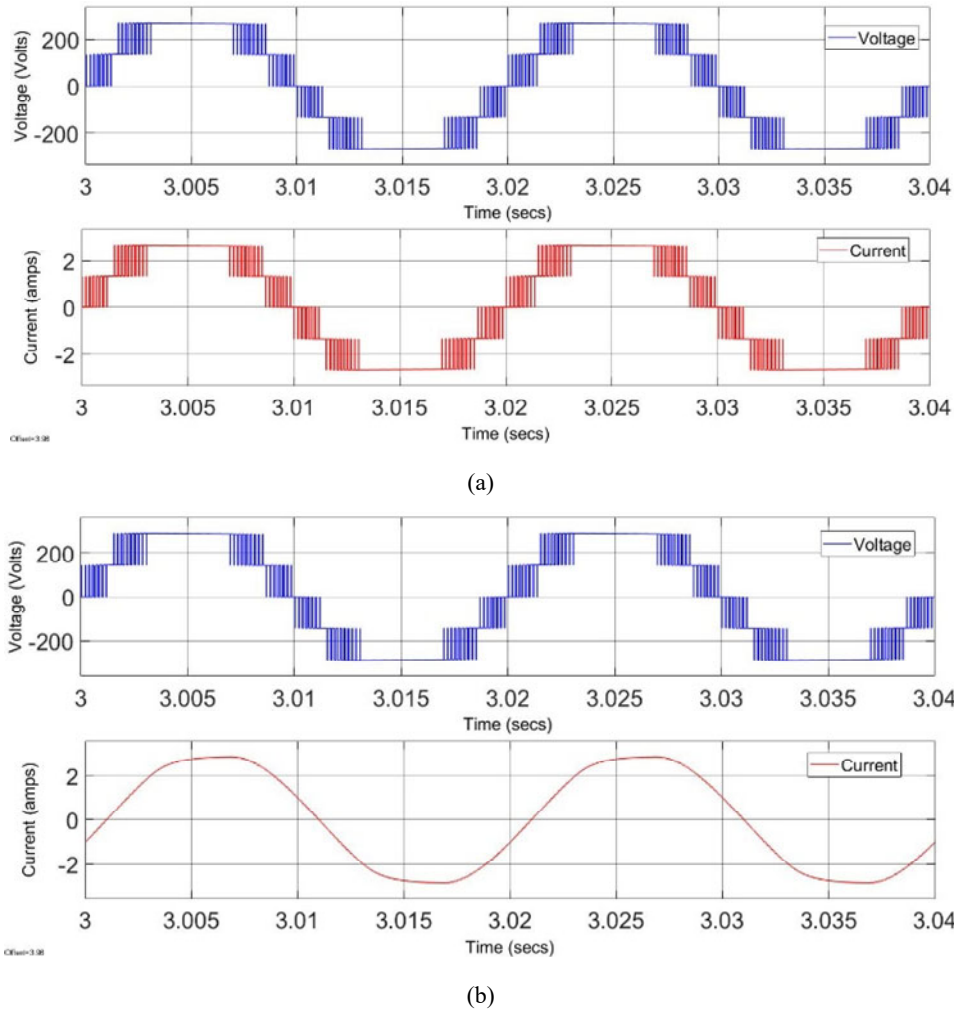


(a)



(b)

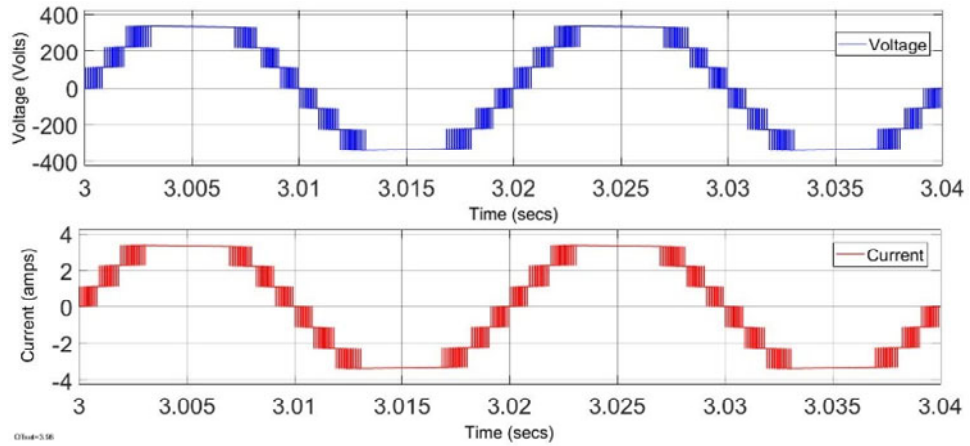
Figure 17 Voltage and current waveform of PV array fed five-level inverter with (a) R load (b) R-L load (see online version for colours)



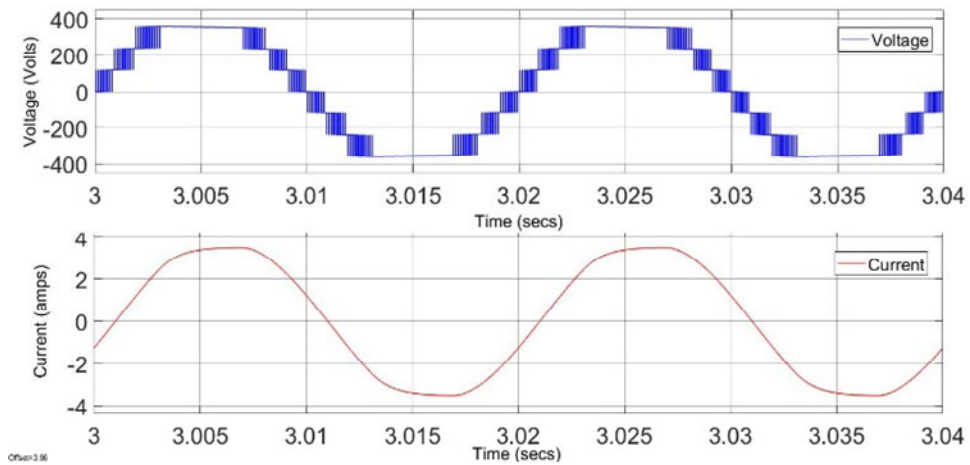
9 Comparative analysis of solar PV fed multi-level inverter

The Analysis of the Solar PV array-fed inverter of various voltage levels shows the presence of THDs in current under different load conditions. Specifically, THDs were observed with an R-load of 100 ohms, drawing current with unity power factor. Additionally, THDs present in an R-L load consisting of 100 ohms and 104.624 mH, as well as in loads with inductors of 154.16 mH and 238.7 mH, drawing current with power factors of 0.95, 0.9, and 0.8 lagging respectively, is shown in Table 7.

Figure 18 Voltage and current waveform of PV array fed seven-level inverter with (a) R load (b) R-L load (see online version for colours)



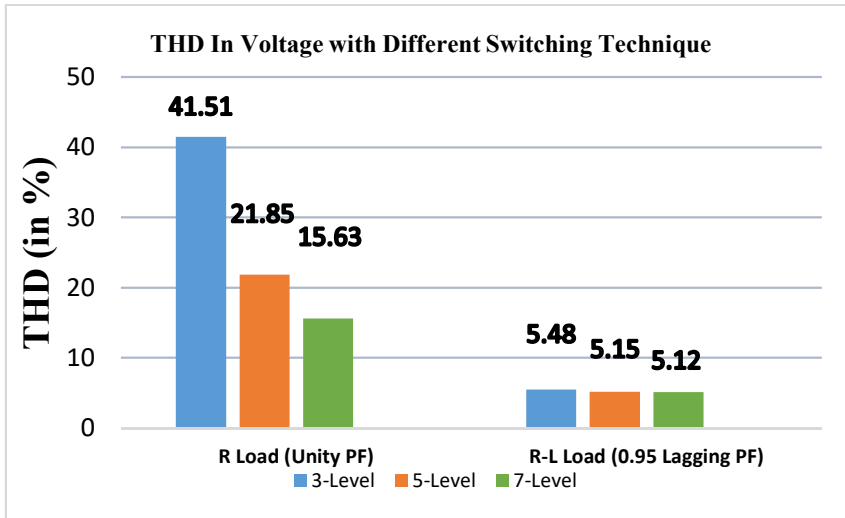
(a)



(b)

Table 7 THD in the current of PV array fed CMLI with R and R-L load

	Power factor	3-level	5-level	7-level
THD in current (in %)	Unity	41.51	21.85	15.63
	0.95 lagging	5.48	5.15	5.12
	0.9 lagging	4.47	4.25	4.22
	0.8 lagging	3.54	3.38	3.34

Figure 19 THD in the current of PV array fed CMLI with R and R-L load (see online version for colours)

10 Conclusions

In this paper, comparative analysis shows the suitability of the PS ST for the solar photovoltaic array-fed inverter. The difference in the performance of the multi-level inverter with the increment of levels and with various multiple-carrier ST has been discussed, with the increment of level in the cascaded inverter, THD in current and voltage decreases. Maximum power extraction from the PV array is possible only at 1000W/m² irradiance and 25-degree temperature. Implementation of all four types of multi-carrier technique in multi-level inverter shows a small difference in THD values but the power consumption of different levels is different in level shifted MC SPWM (PD, POD, and APOD) that may lead to voltage unbalance and unsymmetrical parameter variation in D.C. source. Power consumption of different levels in PS is the same, hence preferred. And it is found suitable for Solar PV applications with a simple control algorithm.

Observation of Solar PV array fed CMLI of three-level, five-level and seven-level shows the presence of 41.51%, 21.85%, and 15.63% respectively with pure resistive load (unity P.F.). With inductive load (0.95 lagging) THD in current reduces to 5.48%, 5.15%, and 5.12% respectively.

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