Programmable FPGA-based 32-channel transmitter for high frame rate ultrasound channel excitation applications

J. Jean Rossario Raj*

Centre for Biomedical Engineering,
Indian Institute of Technology-Delhi,
New Delhi, 110016, India
Email: bmz108120@cbme.iitd.ernet.in
*Corresponding author

S.M.K. Rahman and Sneh Anand

Centre for Biomedical Engineering,
Indian Institute of Technology-Delhi,
New Delhi, 110016, India
and
Biomedical Engineering Unit,
All India Institute of Medical Sciences-Delhi,
New Delhi, 110029, India
Email: rahman@cbme.iitd.ac.in
Email: sneha@cbme.iitd.ac.in

Abstract: This paper describes the design and results of a field programmable gate array (FPGA) designed for ultrasound transient elastography transmitter. The high frame rate is achieved by multi-line transmission. The design is capable of achieving frame rates up to 8,000 frames per second by excitation of all the channels simultaneously. The FPGA also generates the drive signals for the commonly available CMOS transmit pulsers for high voltage excitation of the ultrasound transducer. The FPGA is configured from a microcontroller using a parallel interface. The FPGA also generates the synchronisation pulses for the receiver. The FPGA has a flexible design where parameters like ultrasound frequency, number of pulses per burst, pulse repetition frequency, and so on are programmed from the microcontroller. One FPGA caters for 32 channels and has a maximum frequency of operation of 8 MHz. The novelty of this study is in the design and implementation of an open FPGA architecture for 32 channel high frame rate ultrasound application.

Keywords: field programmable gate array; FPGA; multi-line transmission; MLT; ultrasound scanner; transient elastography.

Reference to this paper should be made as follows: Raj, J.J.R., Rahman, S.M.K. and Anand, S. (2018) 'Programmable FPGA-based 32-channel transmitter for high frame rate ultrasound channel excitation applications', *Int. J. Instrumentation Technology*, Vol. 2, No. 1, pp.18–33.

Biographical notes: J. Jean Rossario Raj is currently doing her research in Centre for Biomedical Engineering, Indian Institute of Technology, Delhi. Her area of research is biomedical signal processing, ultrasound imaging and biomedical instrumentation.

S.M.K. Rahman is an Assistant Professor in Centre for Biomedical Engineering, Indian Institute of Technology Delhi. His research areas include computer architecture, embedded systems; microprocessor based industrial control, digital hardware design and medical electronics.

Sneh Anand is a Professor in Centre for Biomedical Engineering, Indian Institute of Technology Delhi. Her research area includes biomedical instrumentation, rehabilitation engineering, biomedical transducers and sensors, biomechanics technology in reproduction research and controlled drug delivery system. She is the recipient of the IEEE life time achievement award in 2004. She has contributed her 43 years of her life to Indian Institute of Delhi. She optimally combines her engineering training with biomedicine to bring in innovative concepts and give them a practical shape as products which benefit many people in need. With her dedicated biomedical R&D efforts she has published more than 130 papers in reputed biomedical journals. She has eight inventions and four patents to her credit and has transferred eight knowhow to Indian industries.

1 Introduction

Field programmable gate array (FPGA)-based systems offer major advances for parallel computing applications where higher throughput is required. Reprogrammable systems based on FPGAs are revolutionising computation and digital logic. In logic emulation systems, they provide faster computation than software simulation (Hauck, 1998). The objective of this study was to design an FPGA and to develop a prototype for high frame rate ultrasound channel excitation applications. A number of studies were carried out on the application of FPGAs for different application-specific requirements for medical ultrasound scanner applications. Some of these studies are further examined in this paper. A modular low-cost PC-based digital ultrasound imaging system with most of its processing steps done on the PC side with a Virtex-5 FPGA for digital beamforming is presented in Hassan et al. (2011). Use of FPGA as a single chip multi-channel beamformer with digital signal processing provides programming flexibility (Tomov and Jensen, 2001). A pulsed-wave Doppler implementation core with reconfigurable and real-time processing capability using FPGAs is achieved in Hu et al. (2008). The design and experimental results of an FPGA-based real-time ultrasound imaging system that uses a 16-element phased-array capacitive micro-machined ultrasonic transducer fabricated using a fusion bonding process is presented in Wong et al. (2012). The development of an open ultrasound bio-microscopy platform for preclinical studies using FPGA for B-mode imaging and directional pulsed-wave Doppler is presented in Qiu et al. (2012). A programmable architecture for an eight-channel ultrasound transmitter for medical ultrasound research activities with eight transmit channels and an FPGA-based configurable delay profile to steer the acoustic beam, transmit frequency, and pulse pattern length depending on the medical application is presented in Dusa et al. (2014). Platforms with scalability of up to 128 channels and 500 MHz digitalisation for different kinds of applications ranging from low-frequency sonar applications to high-frequency biomedical imaging were studied (Hewener et al., 2012). Such systems were having a single main board mounted with application-specific frontend boards that can be installed for different sampling rates, memory, or processing requirements using Virtex-6 FPGA

and MicroBlaze soft processors, and were highly flexible in terms of waveform generation, modern beamforming programming, and signal processing possibilities

One important application of high frame rate channel excitation, where the current study focuses on the application of FPGAs, is in ultrasound transient elastography for non-invasive qualitative analysis and differentiation of tumours, where frame rates of the order of more than 1,000 fps are required. Earlier developments with ultrasound elastography used low frame rate machines. However, the high frame rate technique is now becoming increasingly popular because of its high accuracy and precision. The high frame rates are achieved through multi-line transmission (MLT) by exciting all the piezoelectric transducers simultaneously. The high frame rate designs become more complex because the data from all the ultrasound channels have to be processed simultaneously, which is complex. Moreover the huge volume of data has to be stored and processed. A hardware design for a transient elastography ultrasound system is presented in Raj et al. (2012a). Several techniques were adopted for the reduction of data volumes in such applications as well. One such method of acquisition of data using a transient window through Ethernet for high frame rate applications is presented in Raj et al. (2015b).

Transient elastography is an emerging technology; the hardware designs used are highly proprietary and details are not available for bringing out newer and cost-effective designs. Ultrasound transient elastography scanners are also available only from a few manufacturers. Hence the technology is not cost-effective for widespread adoption. The availability of modular designs of hardware and software components will make the technology viable and the adoption will be widespread. This study is an attempt to a make the design modular and open. The study was undertaken in two parts, where the modular design was carried out for transmit and receive portions separately. In this part of the study, the core of the transmit portion of the ultrasound transient elastography scanner is presented using an FPGA that is highly modular. In a study presented in Kim et al. (2012), a single FPGA-based portable ultrasound system developed was able to meet the processing requirements in medical ultrasound imaging while providing improved flexibility for adapting to emerging point of care (POC) applications. However, in this study, transmit and receive portions were taken separately because of the simultaneous transmit and receive requirements of large numbers of channels and the subsequent requirement for a large number of inputs/outputs (I/Os). A system that can handle up to 64-element linear array transducers, excite 16 channels, receive simultaneously at a sampling frequency of 100 MHz, and work at a frame rate of 30 fps is presented in a study by Hu et al. (2006). A comparison of the performance parameters for the proposed solution against existing solutions is presented in Table 1.

The study objectives included the FPGA design, which is externally configurable dynamically through a microcontroller for features such as ultrasound frequency, pulse repetition frequency (PRF), number of pulses per burst, and so on. It is also possible to selectively excite the channels for design stage evaluations. The FPGA generated a PRF synchronisation pulse for the receiver to align with the transmitter. The study also evaluated interfacing with different types of CMOS high voltage pulser chips that were commonly available. The design of bipolar pulse generators for dual P-N channel MOSFET and FPGA control is presented in Brown and Lockwood (2002), Wu et al. (2013) and Xu et al. (2007). The high-voltage excitation of the ultrasound transducers has

positive and negative voltage trails generated by paired N-channel and P-channel CMOS devices, which require a positive and negative synchronised excitation sequence. This sequence was generated by the FPGA. One important aspect of the study objective has been to use an external computing device such as a desktop or laptop for the image or data-processing requirements. This step would reduce the cost of the design compared to conventional designs where special-purpose hardware is used for the application.

Table 1 Performance comparison of proposed solution against existing solutions

Parameter	*Existing solutions*	*Proposed solution*
Frame rate of FPGA based designs	50 fps	8,000 fps (maximum)
Frame rate variation	No	Yes from 100 to 8,000 fps
Burst width variation	Yes	Yes
Maximum number of channels per FPGA device	64	32
Flexible channel excitation scheme	No	Yes
Maximum frequency achieved	24 MHz	24 MHz
Ultrasound frequency variation	Yes	Yes
PRF variation	Yes	Yes
Microcontroller control	Yes	Yes
Open design	No	Yes
Cost effective	No	Yes

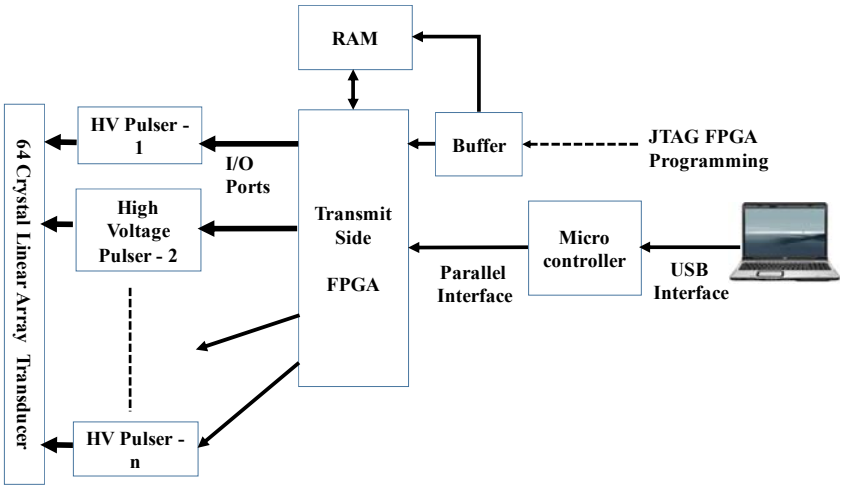
The study presented had many novelties. The study facilitated for the design of a miniaturised ultrasound scanner working at frame rates of the order of 8,000 fps. The FPGA based design helped in introducing soft computing functionalities enabling the image and video processing using external computing device. Ultrasound in general and ultrasound transient elastography in particular is dominated by proprietary designs which make the healthcare technology costly. An open FPGA based architecture was designed and implemented to excite 32 channels simultaneously. The study also presents open interface methods for FPGA with microcontroller and high voltage pulser which could be used for other applications also. This enabled the design and development of a single board, miniaturised hardware for high frame rate ultrasound machine.

2 Materials and methods

2.1 Block schematic of the transmit section

The design requirements for the transmit FPGA have been assessed from the typical block schematic of the transmit section of an ultrasound scanner. The typical block schematic is given in Figure 1. The transmit section consists of microcontroller-based control by the external laptop/computer through a USB interface, high voltage pulsers for generating the required excitation of the transducer array, and the FPGA core for generation of the required controlled and synchronised impulses for the pulsers. The graphical user interface (GUI) is developed in MATLAB, which runs on the laptop.

Figure 1 Block schematic of the transmit section (see online version for colours)



The microcontroller interfaces with the laptop over the USBXpress application programming interface (API). The microcontroller interfaces with transmit and receive FPGAs, analog-to-digital converters (ADC), gigabit Ethernet controller, and gigabit Ethernet physical interface devices. The microcontroller interface required a parallel address and data interface to the FPGA for passing controls from the MATLAB GUI of the laptop. A simple parallel interface was selected, as sufficient interface pins were available in the FPGA and microcontroller. The CMOS pulser generates the high-voltage excitation. The pulser requires positive and negative excitation pulses for the N-CMOS and P-CMOS devices. The output voltage levels are controlled by the input high-voltage supplies, which can be a maximum of ±100 V. In the design, ± 40 V was used. The pulser can operate in pulsed as well as continuous mode (Doppler). This requires suitable current mode inputs to be set for the pulser. Accordingly, the interface with the high voltage (HV) pulser is required to generate the positive and negative CMOS gate drive pulses, enable and disable the pulser device, set the control for the current mode, and so on.

The FPGA has a JTAG interface for the programming headers. The FPGA programming involves the associated external RAM and the buffer. The buffer performs the level translations of the data received by the FPGA. The buffer interface with the FPGA/RAM has the clock and data-in/data-out signals. While programming, the host computer writes the program to the FPGA RAM. During the power-on condition, the FPGA reads the program from the RAM and executes the code. A prototype has also been made for evaluation of the FPGA design using the block schematic in Figure 1.

2.2 Choosing the FPGA

For logic emulation systems, an FPGA provides faster computation compared to software simulation. The logic designs are customised for high performance in different types of applications. In a multimode system, an FPGA yields significant hardware savings and provides generic hardware. Each channel requires four I/Os and the pulser requires enable- and current-mode selections. Thus each eight-channel pulser requires 36 I/Os

from the FPGA. In order to meet the above requirements, a Xilinx FPGA Spartan 3E (XC3S500E_208) with the following specifications is chosen. The FPGA has 172 I/O pins and 216K blocks of internal RAM. Low voltage differential signalling (LVDS) is used for interfacing with the high voltage pulser and receiver chips. The speed of the IO Bus is 622 Mbps, with EEPROM having master-slave/JTAG programming headers.

2.3 FPGA programming requirements

FPGAs contain an array of programmable logic blocks and a hierarchy of reconfigurable interconnections. These blocks can be wired together in different configurations through software logic functions. These logic blocks carry out complex combinational functions. Thus for the development of the software logic, the functional programming requirements for the FPGA were assessed and are given below.

1 The ultrasound frequency selected decides the depth of penetration. Depending upon the scanning requirements, different ultrasound frequencies are required for the channel excitation. This requires the selection of an ultrasound frequency from 2 to 8 MHz.

2 During an ultrasound excitation, multiple pulses are sent as a burst into the scanning area of interest. The intensity of the ultrasound pulse wave is varied by changing the number of pulses per burst. This requires the selection of the number of pulses per burst from say 8 to 32.

3 Variation of the PRF from 1 to 8 KHz also helps to change the depth of penetration. In addition, in the high frame rate design used in this study, the maximum frame rate achievable is the PRF and hence the FPGA design was for a frame rate of 8000 fps.

4 Selective excitation of the channels was required for evaluation purposes; that is, it was necessary to excite any combination or all of the 32 channels at the same time. In high frame rate mode, all the 32 channels were excited simultaneously.

The above functional requirements were classified into the following categories of programming requirements.

1 microcontroller interface program

2 high-voltage pulser interface program

3 logic for the generation of high-voltage excitations.

2.4 Microcontroller-FPGA interface using address/data bus

In the developed prototype, the microcontroller configures the different chips like transmit and receive FPGA, ADCs, gigabit Ethernet controller, gigabit Ethernet physical device, and so on. The microcontroller is interfaced with the MATLAB GUI using a USB interface. The microcontroller firmware implements the USB interface logic to an external computing device as well as the interface logic for the other internal chips. A block schematic of the microcontroller-FPGA interface is given in Figure 2. The microcontroller interface consists of an eight-bit address bus, an eight-bit data bus, read, write, and chip-select controls. Chip select is used for selective read or write operations

over a parallel bus as both transmit and receive FPGAs are connected over the same address/data bus. The read and write controls are for informing the slave device, that is, the FPGA, that the master is going to perform a read or write operation.

Figure 2 Block schematic of the microcontroller-FPGA address/data bus interfacing (see online version for colours)

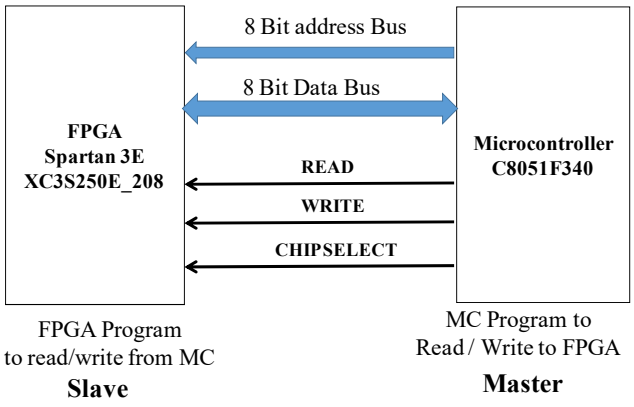
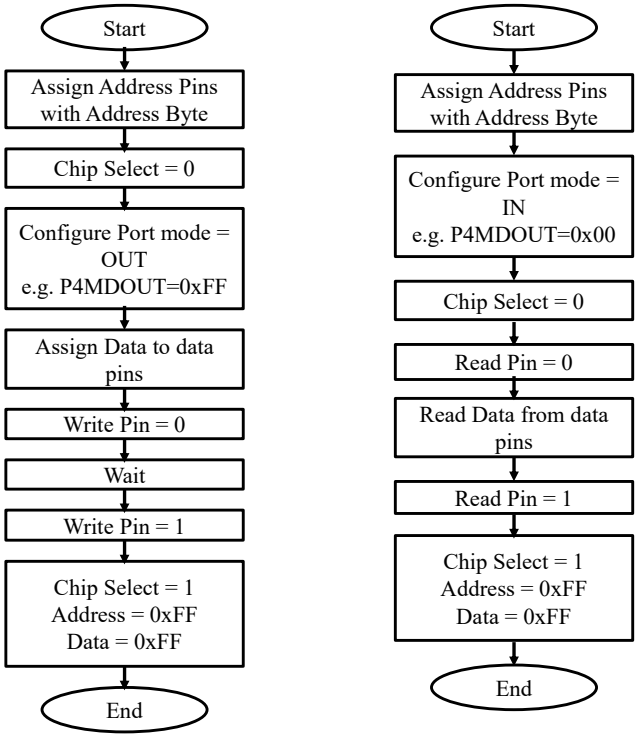


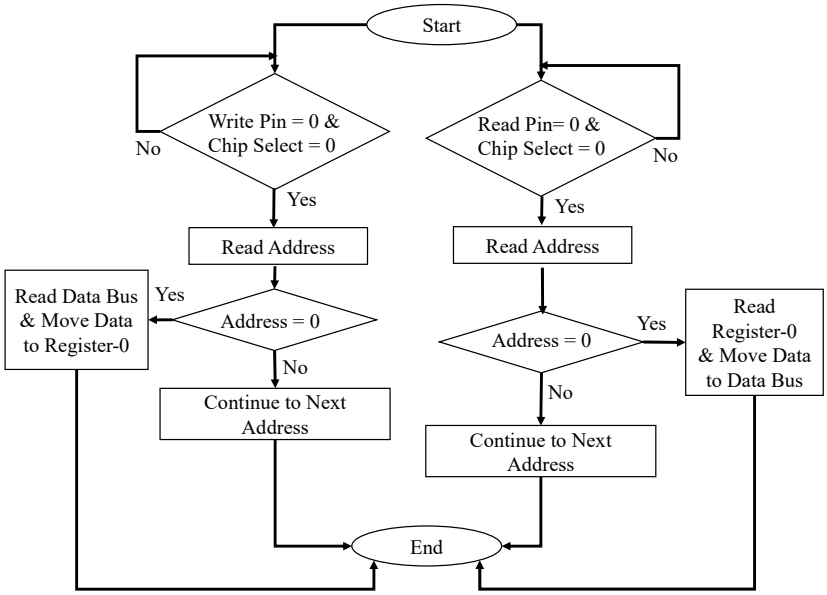
Figure 3 Flow chart of microcontroller firmware for address/data bus interfacing: write and read operations



The flowchart of the microcontroller firmware for the read and write operations is given in Figure 3. The microcontroller program is written in 'C' language. During the read/write operation, the selected FPGA's chip select is set to logic low level. This will initiate the FPGA for the write/read operation. P4MDOUT is used to assign the respective port of the microcontroller in the read or write mode. In the write operation, during the period when the write pin = 0, the FPGA reads the information from the address and data pins. Similarly, when the microcontroller read pin = 0, the FPGA reads the address bus, fetches the data corresponding to the address, and places the data in the data bus and the microcontroller reads the data.

The FPGA program is written in VHSIC hardware description language (VHDL). The flow chart of the FPGA-side program for address/data bus interfacing is given in Figure 4. The FPGA operation starts when the chip select becomes low, that is, during the falling edge of the chip select. In the write operation, when the write pin = 0, the FPGA reads from the microcontroller bus and writes to the corresponding FPGA register. While writing into the register, the data are fed to all the registers and only the corresponding register address matching the input address is enabled. In the read operation, when the read pin = 0, the FPGA reads the address from the microcontroller bus and the data corresponding to the address register are placed in the microcontroller data bus.

Figure 4 Flow chart of FPGA program for address/data bus interfacing

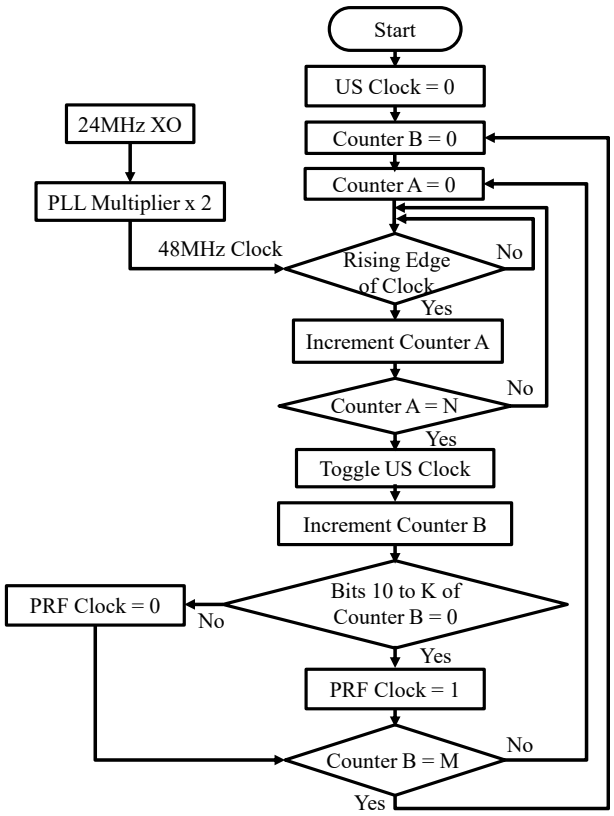


2.5 FPGA algorithm for high frame rate excitation

The high frame rate is achieved by exciting all the channels at the same time. The high-voltage pulser to be enabled or the channels to be excited are controlled by the microcontroller by writing into different FPGA registers. Accordingly, the FPGA can generate an excitation sequence for the selected channels. The flow chart of the firmware

for high frame rate excitation is given in Figure 5. The FPGA uses a 24-MHz crystal oscillator for generation of the master clocks. Internally, in the FPGA, a phase locked loop (PLL) multiplier (doubler) converts this clock to 48 MHz. The FPGA generates the ultrasound frequency with a selected number of pulses repeated at the PRF. In this clock, the illustration is made using 8-MHz ultrasound frequency, eight pulses per burst, and 8-KHz PRF.

Figure 5 Flow chart of FPGA algorithm for all crystal excitations



The FPGA logic uses two counters, A and B. Counter A generates an 8-MHz clock by toggling between one and zero using the divide-by-three counter. By changing the depth of this counter, different ultrasound frequencies were generated. Counter B counts to 2,000 for 8-KHz PRF. Similarly the depth of this counter is varied for different PRFs. During the counter B counts, the output is set to logic high level during a specific number of counts, such as eight in this case, for the specific number of bursts. That is, the output pulse is sent until the Kth bit position of the counter reaches '1'. The value of 'K' is changed for different burst widths. The logic was tested for different ultrasound frequencies, burst widths, and PRFs. The counter value limits for a PRF of 8 KHz are given in Table 2. Table 3 indicates the bit control for generation of the required pulse burst.

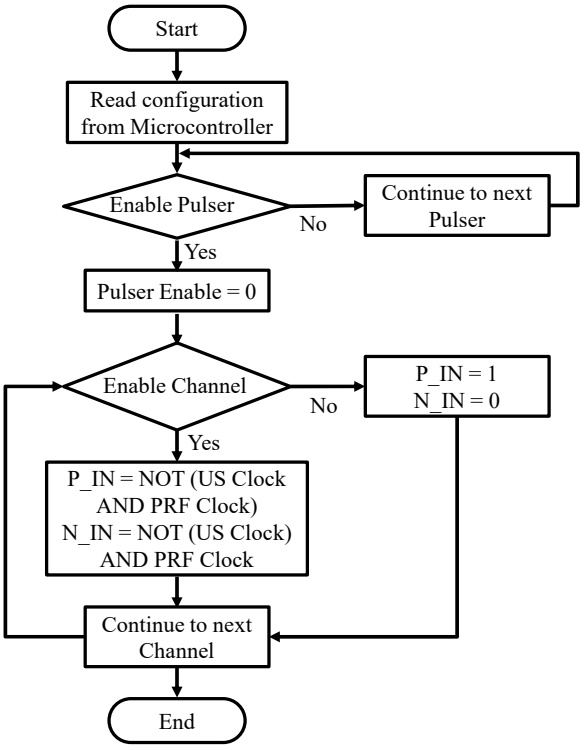
Table 2 Counter A and B limits for 8-KHz PRF and different ultrasound frequencies of operation

Ultrasound frequency (MHz)	*N*	*M*
8	3	2,000
6	4	1,500
4.8	5	1,200
4	6	1,000
3	8	750
2	12	500

Table 3 Control of pulses per burst in the flow chart in Figure 5

Number of pulses per burst	*K*
8	4
16	5
32	6

Figure 6 FPGA algorithm for CMOS pulser interfacing



2.6 FPGA interface with high-voltage CMOS pulsers

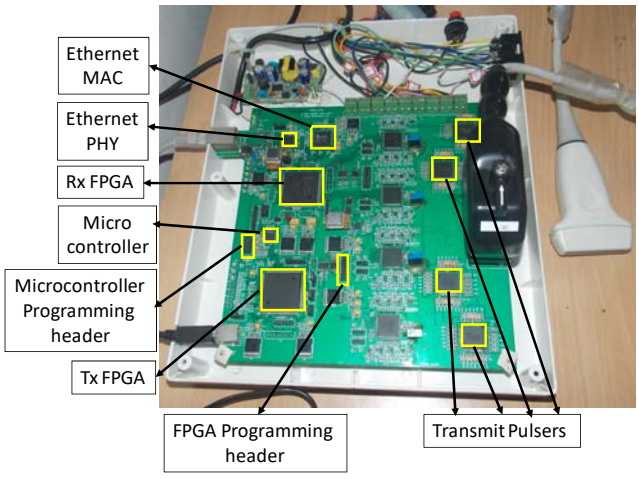
This logic enables the high-voltage pulser by generation of the excitation gate pulse for the P-channel and N-channel CMOS devices of the HV pulser. The flow chart of the logic is given in Figure 6. The 32 channels are individually enabled by the microcontroller. Hence each channel can be individually excited or a group of channels or all the channels can be excited. The HV pulser chip is also enabled depending upon whether its channels are ON or OFF. The channels and the pulser chips to be enabled are based on the register values configured by the microcontroller.

The output pulse trail is generated using the 8-MHz (typical) ultrasound frequency clock as well as the PRF clock. The PRF clock is ON for the required burst width period; that is, at eight bursts, the PRF clock is ON for 1 µs (8 × 125 ns) and OFF for 125 µs. [NOT (US clock AND PRF clock)] will generate the positive trail whereas [NOT (US clock) AND PRF clock] will generate the negative trail.

3 Results

A prototype developed for the ultrasound scanner with a USB interface to the MATLAB GUI is shown in Figure 7. The prototype has a Silicon Laboratories C8051F340 microcontroller, Xilinx FPGAs, high-voltage pulser from Hitachi, and ADCs (AD9272) from analogue devices. It has the microcontroller and FPGA programming headers as well as the USB interface. The important chips are marked in the figure. The scanner data are received through the Ethernet interface.

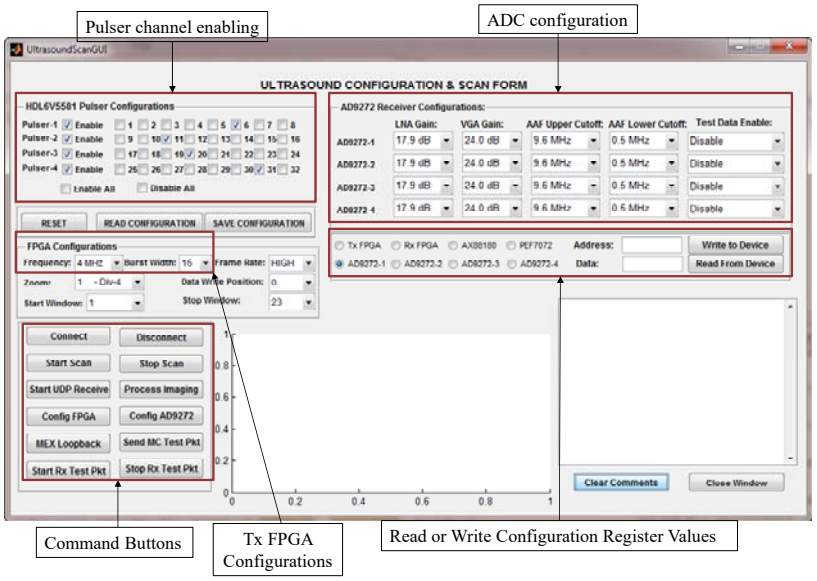
Figure 7 Ultrasound scanner prototype hardware (see online version for colours)



The MATLAB GUI is shown in Figure 8. The configuration of the various ADC's, FPGA and gigabit Ethernet physical interface device (PHY) are performed from this GUI. The AD9272 configurations include the LNA gain, variable gain amplifier (VGA) gain, anti-aliasing filter (AAF) upper and lower cut-off frequencies, enabling/disabling of different test patterns, and so on. The enabling of different ultrasound channels is

performed by configuring the pulsers through the microcontroller and Tx FPGA. The ultrasound frequency and burst width are also programmed from the GUI as shown in Figure 8. The various register values in these devices are also read and written through this interface for the purpose of testing.

Figure 8 MATLAB GUI for configuration of various scanner parameters (see online version for colours)



The output pulse waveform generated by the prototype is shown in Figure 9 with eight pulses. The positive and negative trials of the waveform are also shown. The amplitude of the output pulse is controlled by the voltage levels from the power supply unit. In continuous wave mode, amplitude of ±5 V is used, whereas in pulsed mode, amplitude of up to ±100 V can be used. However in the prototype, ±40 V is used. The ultrasound frequency, pulses per burst, pulse width, PRF , and so on are programmed from the GUI. The variation of ultrasound pulse width based on ultrasound frequency and number of pulses per burst for two typical ultrasound frequencies of 8 and 2 MHz are given in Table 4.

Table 4 The variation of ultrasound pulse width, ultrasound frequency, and number of pulses per burst

Ultrasound frequency (MHz)	*Pulses per burst*	*Pulse width (µs)*
8	8	1
	16	2
	32	4
2	8	4
	16	8
	32	16

Finally, the starting and stopping of scanning by the device are also controlled through the microcontrollers by configuration of the FPGAs in transmit and receive directions. A phantom using agar-gelatin material was prepared in the laboratory for the evaluation of the developed prototype. A scan image captured using the prototype is given in Figure 10 using a 64-channel linear array ultrasound probe. In the end-user perspective, the important pin-outs for the FPGA are indicated in Table 5.

Table 5 FPGA pin-out architecture

Function	*Pins used*
Input control for high voltage PMOS	32
Input control for high voltage NMOS	32
Drive current mode control for the pulser	8
PMOS logic input polarity control	4
High voltage pulser enable	4
Microcontroller address bus	8
Microcontroller data bus	8
Microcontroller chip select, read write controls	3
Clock input	2
LED indications	32
Synchronising clock output	1
Power	24
Ground	20

Figure 9 Output pulse waveform based on microcontroller FPGA control (see online version for colours)

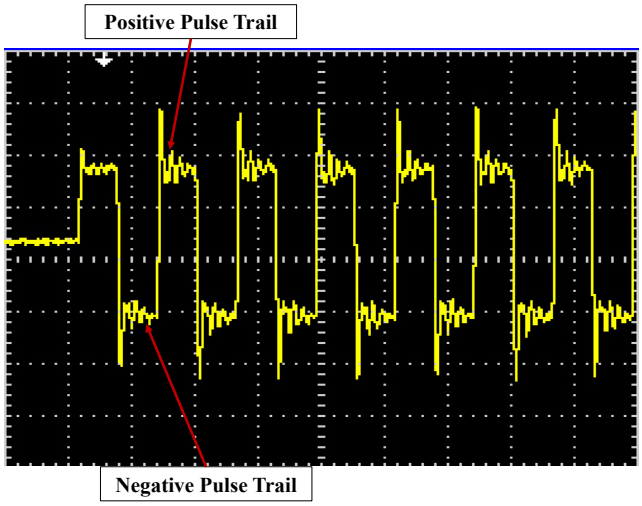
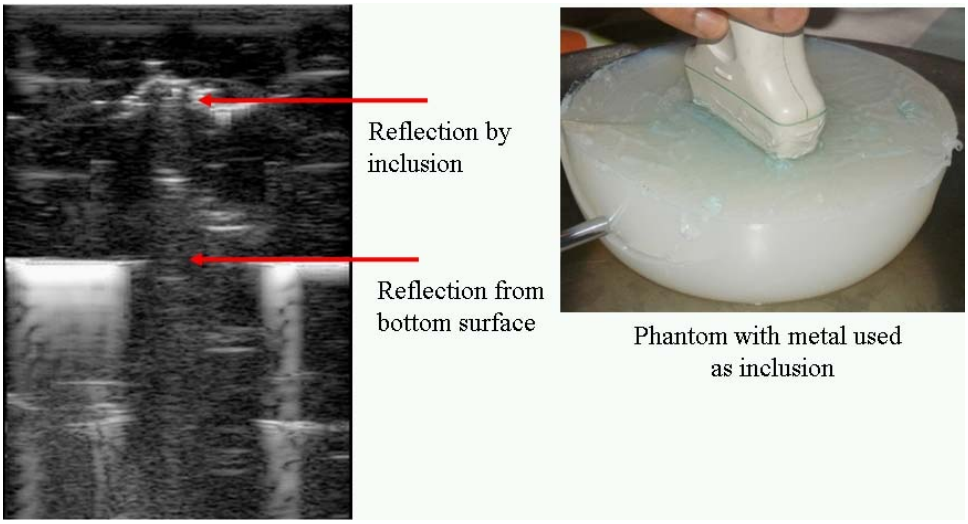


Figure 10 The ultrasound scanner output with phantom (see online version for colours)



4 Conclusions and discussion

The study has been conducted as a part of the development of a prototype for high frame rate ultrasound applications. This technique is prominently used for the transient elastography ultrasound technique for the detection of elasticity of tissues. Accordingly the study involved the design of receive FPGA studied in Raj et al. (2016c), microcontroller to FPGA interfacing studied in Raj et al. (2016a), microcontroller to USB interfacing studied in Raj et al. (2016d), development of the embedded system studied in Raj et al. (2012b) and the elasticity estimation studied in Raj et al. (2016b). The prototype design shown in Figure 7 is the result of all these studies. Thus the developed prototype was able to estimate the elasticity using high frame rates. This prototype was miniaturised and cost effective as compared with the existing designs available in the market.

The study has yielded the following outcomes. The design gave a flexible architecture vis-à-vis application specific designs available. Most of the designs available in the market are for either for low frame rate or high frame rate applications. However this design yielded a flexible architecture for both low and high frame rate applications with single, group and all transducer element excitations. The design is limited to 32 channels because of the limitation of the number of pin-outs of the FPGA chip used. However if higher class of FPGA's i.e. Virtex series etc., is used, the design can be used for 64 or 128 transducer element applications. FPGA design uses general purpose hardware which is cost effective compared to application specific integrated circuits (ASIC). Microcontroller interfacing with the FPGA's yielded full flexibility and control on the design configurations for the present and future requirements. The control is achieved by

configuring the various parameters in the FGPA registers by the microcontroller. Also additional registers have been positioned to meet the future requirements. The approach is able to interface with CMOS high voltage pulsers of different makes depending upon the chip requirements. Accordingly the pin-outs of the FPGA given in Table 5 will enable the future users to use this design for their applications.

ASICs have been traditionally used to support the high computational and large data rate requirements in medical ultrasound systems, particularly in beamforming. The results achieved in this paper indicate that this programmable architecture can meet the requirements of low- and medium-level ultrasound machines while providing a flexible platform for supporting the development and deployment of new algorithms and emerging clinical applications. The usage of high frame rate ultrasound machines is very limited mainly in large cities because of the limited technologies and huge investment requirements. Hence this is a challenge in tele-medicine applications too. However, this development has helped in the miniaturisation of the design of the ultrasound machine for high frame rate applications and has thus helped in the development of an ultrasound machine suited for tele-medicine applications (Raj et al., 2015a).

This interfacing has wider implications in other areas of microcontroller control programming and is hence a very innovative approach. This programmable ultrasound machine will not only offer significant advantages in terms of its low cost, portability, scalability, and reduced development time but also provide a flexible platform for developing and deploying new clinical applications to aid clinicians and improve the quality of healthcare offered to patients. It also has many applications in areas of sensors including medical electronics.

References

Brown, J.A. and Lockwood, G.R. (2002) 'A low-cost, high-performance pulse generator for ultrasound imaging', *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 49, No. 6, pp.848–851 (accessed 2002).

Dusa, C., Rajalakshmi, P., Puli, S., Desai, U. and Merchant, S. (2014) 'Low complex, programmable FPGA based 8-channel ultrasound transmitter for medical imaging researches', *e-Health Networking, Applications and Services (Healthcom), 2014 IEEE 16th International Conference on*, IEEE, pp.252–256.

Hassan, M., Youssef, A-B.M. and Kadah, Y.M. (2011) 'Modular FPGA-based digital ultrasound beamforming', *Biomedical Engineering (MECBME), 2011 1st Middle East Conference on*, IEEE, pp.134–137.

Hauck, S. (1998) 'The roles of FPGAs in reprogrammable systems', *Proceedings of the IEEE*, Vol. 86, No. 4, pp.615–638 (accessed 1998).

Hewener, H.J., Welsch, H-J., Fonfara, H., Motzki, F. and Tretbar, S.H. (2012) 'Highly scalable and flexible FPGA based platform for advanced ultrasound research', *Ultrasonics Symposium (IUS), 2012 IEEE International*, IEEE, pp.2075–2080.

Hu, C-H., Xu, X-C., Cannata, J.M., Yen, J.T. and Shung, K.K. (2006) 'Development of a real-time, high-frequency ultrasound digital beamformer for high-frequency linear array transducers', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 53, No. 2, pp.317–323 (accessed 2006).

Hu, C-h., Zhou, Q. and Shung, K.K. (2008) 'Design and implementation of high frequency ultrasound pulsed-wave doppler using FPGA', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 55, No. 9, pp.2109–2111 (accessed 2008).

Kim, G-D., Yoon, C., Kye, S-B., Lee, Y., Kang, J., Yoo, Y. and Song, T-K. (2012) 'A single FPGA-based portable ultrasound imaging system for point-of-care applications', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 59, No. 7, pp.1386–1394 (accessed 2012).

Qiu, W., Yu, Y., Tsang, F.K. and Sun, L. (2012) 'An FPGA-based open platform for ultrasound biomicroscopy', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 59, No. 7, pp.1432–1442 (accessed 2012).

Raj, J., Rahman, S. and Anand, S. (2015a) 'Interfacing high frame rate data through ethernet without loss for tele-medical applications', *Signal Processing and Communication (ICSC), 2015 International Conference on*, IEEE, pp.51–55.

Raj, J.J.R., Rahman, S. and Anand, S. (2015b) 'Acquisition of lossless data in transient window through ethernet in high frame rate machines', *Computing for Sustainable Global Development (INDIACom), 2015 2nd International Conference on*, IEEE, New Delhi, pp.591–596.

Raj, J., Rossario, J., Rahman, S. and Sneh, A. (2012a) 'Electronic hardware design for ultrasound transient elastography', *International Journal of Engineering Science and Technology*, Vol. 4, No. 8, pp.3700–3704 (accessed 2012).

Raj, J.R., Rahman, S.M.K. and Anand, S. (2012b) 'Electronic design of compact power supply unit for various voltages in ultrasound transient elastography', *International Journal of Electronics Communication and Computer Engineering*, Vol. 3, No. 4, pp.896–900 (accessed 2012).

Raj, J.R., Rahman, S.M.K. and Anand, S. (2016a) '8051 microcontroller to FPGA and ADC interface design for high speed parallel processing systems – application in ultrasound scanners', *Engineering Science and Technology, an International Journal*, Vol. 19, pp.1416–1423.

Raj, J.R., Rahman, S.M.K. and Anand, S. (2016b) 'FPGA based embedded system for high frame rate ultrasound with ethernet interface', *Journal of Medical Imaging and Health Informatics*, Vol. 6, No. 3, pp.1–10.

Raj, J.R., Rahman, S.M.K. and Anand, S. (2016c) 'FPGA design for multi-line acquisition & ethernet interface in high frame rate ultrasound machines', *IETE Journal of Research*, pp.1–8.

Raj, J.R., Rahman, S.M.K. and Anand, S. (2016d) 'Microcontroller USB interfacing with MATLAB GUI for low cost medical ultrasound scanners', *Engineering Science and Technology, an International Journal*, Vol. 19, pp.964–969.

Tomov, B.G. and Jensen, J.A. (2001) 'A new architecture for a single-chip multi-channel beamformer based on a standard FPGA', *Ultrasonics Symposium, 2001 IEEE*, IEEE, pp.1529–1533.

Wong, L.L., Chen, A., Logan, A.S. and Yeow, J.T. (2012) 'An FPGA-based ultrasound imaging system using capacitive micromachined ultrasonic transducers', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 59, No. 7, pp.1513–1520 (accessed 2012).

Wu, J-X., Du, Y-C., Lin, C-H., Chen, P-J. and Chen, T. (2013) 'A novel bipolar pulse generator for high-frequency ultrasound system', *Ultrasonics Symposium (IUS), 2013 IEEE International*, IEEE, pp.1571–1574.

Xu, X., Yen, J.T. and Shung, K.K. (2007) 'A low-cost bipolar pulse generator for high-frequency ultrasound applications', *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, Vol. 54, No. 2, pp.443–447 (accessed 2007).