# Elimination of output gating performance overhead for critical paths in scan test

Ashok Kumar Suhag*

Gautam Buddha University,
Greater Noida, 201312, India
E-mail: ashoksihag@gmail.com
*Corresponding author

Satdev Ahlawat

Indian Institute of Science,
Bangalore, 560012, India
E-mail: satdev.ahlawat@gmail.com

Vivek Shrivastava

National Institute of Technology,
Delhi, 110077, India
E-mail: shvivek@gmail.com

Nidhi Singh

Gautam Buddha University,
Greater Noida, 201312, India
E-mail: nidhisafya@gmail.com

**Abstract:** Excessive switching activity in test mode results in higher power dissipation than normal mode of operation and becoming a serious issue, in order to avoid reliability problems. Scanning of test vectors in test mode causes unnecessary switching in combinational block which can be reduced by gating methods. Gating the outputs of scan cells is a recently proposed very efficient low power test technique, which reduces the scan shift power significantly. However, the output gating techniques impacts the performance severely. In this paper, we propose a modified transistor level design of a scan flip-flop for critical paths, which eliminates the unnecessary switching in combinational circuit during shift phase of a scan-based test, without the impact on performance as in earlier scan flip-flop output gating schemes (Khatri and Ganeshan, 2008). The new scan flop design not only eliminates the performance overhead of output gating but also improves the performance of the scan flop by 32.84% (Khatri and Ganeshan, 2008) and 11.5% (Yang et al., 2008). The new flip-flop disables the output and uses an alternate path for shifting the test vectors. This approach have area overhead of six extra transistors but improves the overall performance of scan flip-flop, so this approach is better suited for critical paths. This also allows us to increase the shift frequency in designs where shift power dissipation puts upper bound on the frequency, and hence reduces test application time.

**Keywords:** scan-based testing; scan flip-flop; low power testing; launch on capture; launch on shift; timing critical path.

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**Biographical notes:** Ashok Kumar Suhag is pursuing his PhD in VLSI Testing from School of Engineering, Gautam Buddha University, Greater Noida. He received his MTech in Microelectronics and VLSI Design from Kurukshetra University, India in 2008 and BE in Electronic Instrumentation and Control from Rajasthan University, India in 2005. His research interests include computer-aided design and test, design for testability and delay fault testing.

Satdev Ahlawat obtained his Master's degree from the Department of UCIM, Panjab University Chandigarh, India in 2010. He is currently working as a Lecturer at Kurukshetra University, Kurukshetra. His current research focuses on design for test and power aware testing of complex VLSI circuits.

Vivek Shrivastava is currently Associate Professor and Academic in charge at National Institute of Technology Delhi. He completed his BTech in Electrical Engineering from RGPV Bhopal and PhD from Indian Institute of Technology Kharagpur. He had carried out industrial assignment at SanDisk Semiconductors at Shanghai and USA. He has published more than 25 papers on system reliability, probabilistic power system planning and test analysis in reputed international journals and conferences. He is a member of IETE India and IEEE USA.

Nidhi Singh obtained her BTech in Electrical Engineering from GJ University Hissar in 1996 and MTech in Control Engineering from REC Kurukshetra in 2001. She received her PhD in Electrical Engineering from IIT Roorkee in 2008. Currently, she is working as an Assistant Professor in Electrical Engineering Department, School of Engineering, Gautam Buddha University, Greater Noida, India. Her research interests are in the area of optimisation, control, and model order reduction of large scale systems.

## 1 Introduction

Power consumption during scan-based testing is much more in test mode than in normal mode due to higher switching activity (Zorian, 1993; Rajski and Tyszer, 1998; Girard, 2000; Nicolici and Al-Hashimi, 2003). The elevated power dissipation in test mode causes several problems such as reliability problems, permanent circuit damage, increased product costs, performance degradation, reduced battery lifetime in case of portable devices that includes BIST architecture for periodic self-testing, and decreased overall yield (Bushnell and Agrawal, 2000). In test mode power is consumed both in combinational and sequential block in the circuit under test. When scan values are loaded inside a scan chain, the value of scan ripple propagates to the combinational block and redundant switching occurs in the gates during the entire scan-in/out period. The low correlation between consecutively applied test vectors and there response produces more transitions than in functional mode. It is observed that 78% of total test power is

dissipated in the combinational logic alone (Gerstendrfer and Wunderlich, 1999). Hence, a low power scan design should address techniques to reduce redundant power in the combinational block during test application.

Majority of the existing research focuses on algorithms that use test vector reordering (Tudu et al., 2009a) or scan chain reordering (Bonhomme et al., 2002; Dabholkar and Chakravarty, 1994) to reduce the power consumption. Algorithmic methods also include X-filling (Butler et al., 2004; Kajihara et al., 2002), low transition ATPG (Wang and Gupta, 2002) and multiple scan chain technique (Bonhomme et al., 2006; Whetsel, 2000). Tudu et al. (2009a) determined the minimum achievable peak power during test for a given test vector set and use test vector reordering to support the minimum achievable peak power. Tudu et al. (2009c) used test vector reordering to reduce the peak power by reducing capture power when capture cycles of various cores coincides in SOCs. Similarly in Tudu et al. (2009b), a graph theoretic problem formulation for scan chain reordering is shown for peak power minimisation as the objective. In Whetsel (2000), Whetsel provided a solution for reduction in average and peak power dissipation by transforming conventional scan architecture into desired number of selectable, separate scan paths, and activates these segments one at a time using different enable lines to reduce power consumption due to scan shifts, without increasing the test application time. Another method to achieve power reduction involves output gating in stimulus path of flip-flops to prevent propagation of scan ripple effect to logic gates. The gating of flip-flop offers a simple and effective solution to significantly reduce test power, independent of test set. Gerstendrfer and Wunderlich (1999) have proposed NAND [Figure 2(a)] or NOR gate-based output blocking techniques. The blocking gates are controlled by scan enable signal and the stimulus paths remain freeze at either logic '0' or logic '1' during the entire scan shift operation. However, it increases the delay in the critical path thereby reducing the performance. In Khatri and Ganeshan (2008), the authors use a transmission gate followed by a pull-up or pull down transistor to gate the Q output and maintain it to a constant logic value of 1 or 0. The structure of such a scan flop gated by a transmission gate is shown in Figure 2(b). Parimi and Sun (2004) proposed a modified scan cell with an extra latch. The extra latch maintains a constant value at the inputs of the combinational part of the CUT during shift phase. Although these methods eliminate the average dynamic power dissipated by the combinational part of the CUT during scan in/out, the gating logic introduces circuit performance degradation as well as high area overhead. The main drawback of the output gating technique is performance overhead caused by the blocking logic that falls in the functional path. Zhang et al. have used multiplexers as blocking logic at the output of the scan cells, which hold the previous states of the scan register and thus, prevent activity in combinational logic (Zhang and Roy, 2000). The problem with the multiplexer logic is that it adds significant delay in the signal propagation path from the scan flip-flop to logic. Moreover, they have large overhead in terms of area and switching power in normal operation of circuit. *This motivates to design a scan flip-flop which eliminates the performance overhead due to output gating method*.

The delay penalty due to gating is reduced in ElShoukry et al. (2005), while keeping the power reduction to the desired level, by proper selection of the percentage of gating elements, their position in the scan chain and the output values to hold these gating elements to. It also shows that significant power is consumed in the gating elements themselves, and in all the benchmarks the peak power increased from 5% to 60% when the gating overhead was considered, because of the large switching activity occurring in

the gating logic during scan mode to capture mode. However, due to the large fan-out cones of the flip-flops, un-gated flip-flops can lead to a significant amount of power consumption. Mishra et al. (2010) have proposed a new design of a scan flip-flop which disables the functional slave latch during test mode, replacing it by an alternate redundant low cost dynamic latch. The proposed hardware uses a transmission gate to disable the slave latch that increases the critical path delay. Moreover, the alternate dynamic latch and extra circuitry needed to make the circuit work in both LOS and LOC mode, has large overhead in terms of area. Lin and Rajski (2008) reduced the capture power dissipation by blocking the output of scan cell.

Although this blocking logic comes in function path during normal mode of operation, so it degrades the overall performance.

In this work, we propose a low power scan flop design to eliminate output gating performance overhead for critical paths. The new scan flip-flop not only eliminates power dissipation in combinational circuit during scan shifting but also, improves of the performance of the circuit by reducing the overall delay of critical paths. As the new scan flop targets only the critical paths, the overall area overhead due to the extra circuitry used in the scan flop to eliminate the delay of the output gating logic is marginal. For non-critical paths, transmission gate-based output gating scheme can be used without any performance overhead.

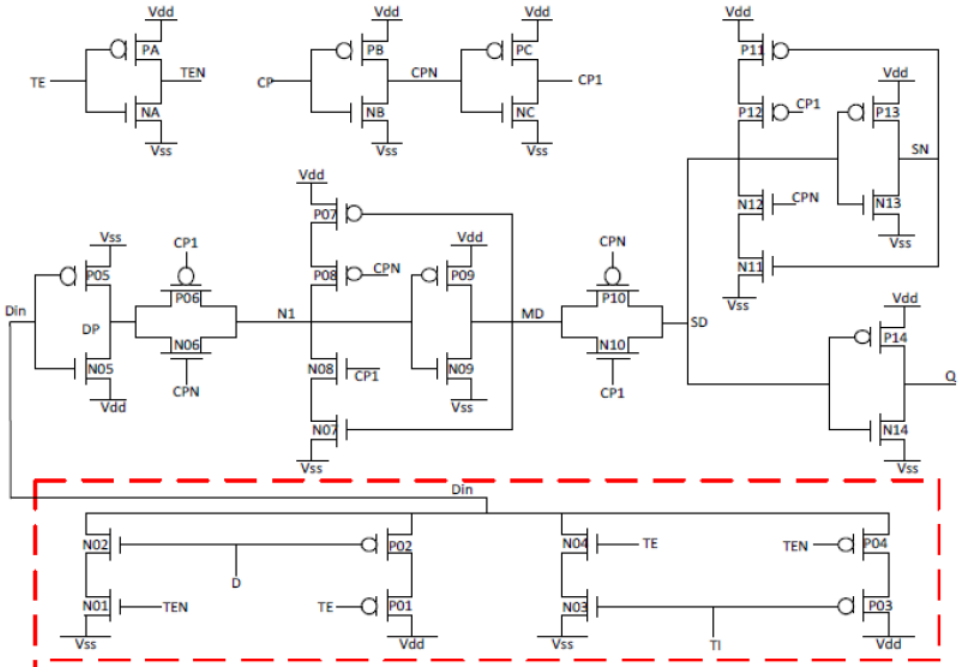
The rest of the paper is organised as follows: Section 2 describes the existing normal scan cell used in this work and the modified scan cell. It explains the details of application of test vectors to the combinational circuit. It also discusses the improvements in performance and scan shifting power reduction. Section 3 contains the experimental results which supports the achieved improvements. Section 4 concludes the paper and also presents the future direction of work.

## 2 Preliminaries and proposed scan flip-flop design

Figure 1 shows transistor level implementation of the considered normal scan cell implementation in this work. This scan cell is based on Power PC 603 MS latch (Stojanovic et al., 1998), which has also been studied by Yang et al. (2008, 2009). Traditionally, a scan flip-flop consists of a master-slave latch pair, connected in series, with muxed input. This scan cell is a positive edge triggered muxed input D flip-flop. In Figure 1, the circuit highlighted by the dashed line (red coloured) rectangle is the multiplexer used for selecting between the functional data in (D) and test scan in (TI) inputs. The circuit between the nodes DP and MD is the master latch of the flip-flop, and the circuit between the node MD and the output (Q) forms the slave latch. When the test enable signal (TE) is set to logic high (‘1’), TI is selected and the circuit operates in test mode. The value of TI then propagates to the master latch when clock (CP) is low. Meanwhile, the nodes in the slave latch retain the values from the previous clock cycle. When CP turns to high, the signal stored in the master latch propagates to the slave latch and to the output of the scan cell. In the same way when the test enable signal (TE) is set to logic low (‘0’), D is selected and the circuit operates in functional mode. As it can be seen from Figure 1, there are two output nodes Q and SQ in the referenced scan cell implementation. The logic level value at both the nodes will be same at any point in time. However, the output Q is used to drive the combinational logic because of the feedback

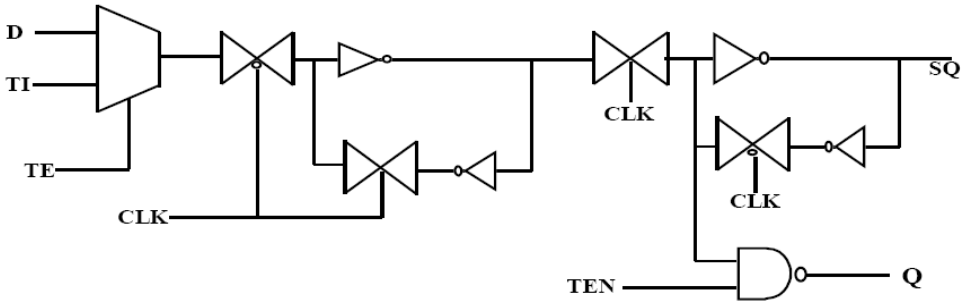
load on the SQ output, which makes that output node slow to drive the combinational logic.

**Figure 1** Transistor level implementation of the considered normal scan flip-flop (see online version for colours)




*Source:* Butler et al. (2004) and Wang and Gupta (2002)

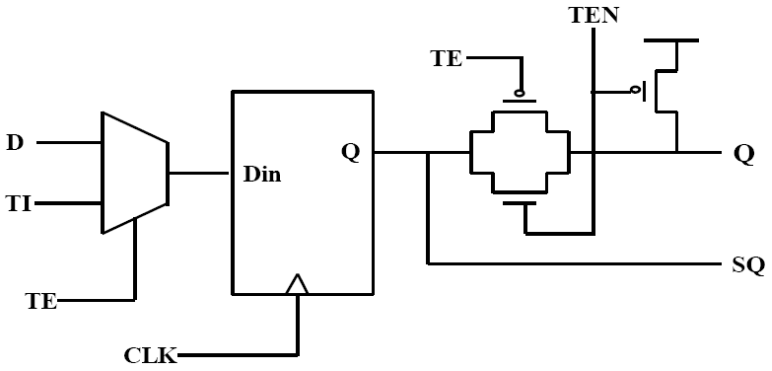
**Figure 2** Scan flip-flop output gating structures, (a) NAND as gating logic (Zorian, 1993) (b) Transmission gate with pull-up




(a)

*Source:* Gerstendrfer and Wunderlich (1999) and Khatri and Ganeshan (2008)

**Figure 2** Scan flip-flop output gating structures, (a) NAND as gating logic (Zorian, 1993) (b) Transmission gate with pull-up (continued)




(b)

*Source:* Gerstendrfer and Wunderlich (1999) and Khatri and Ganeshan (2008)

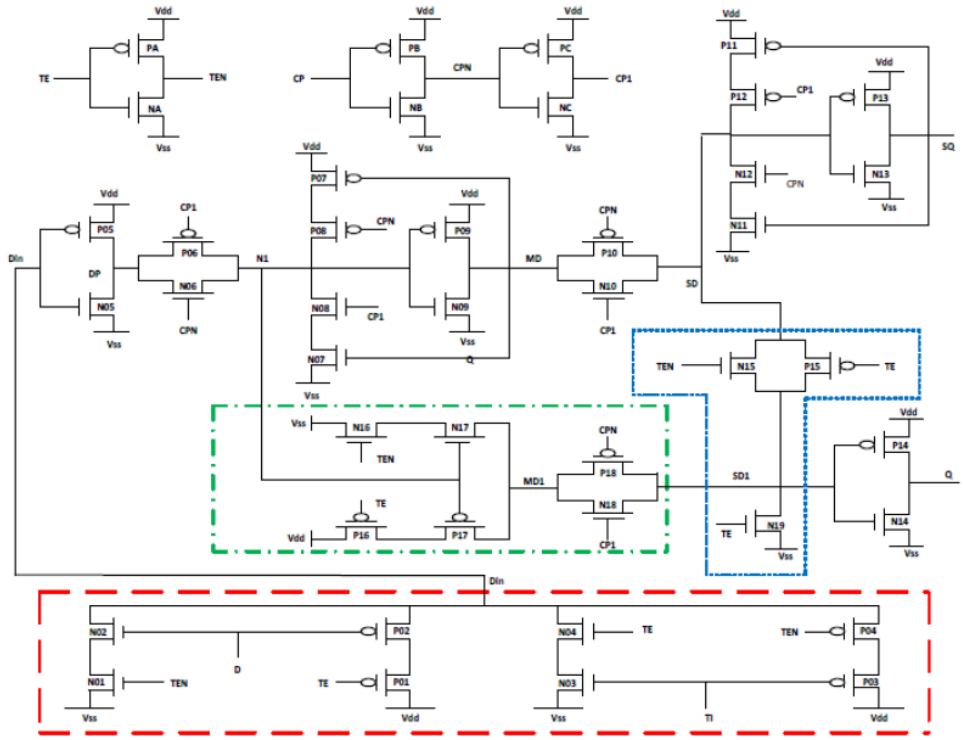
## *2.1 Proposed transistor level scan flip-flop design*

In this work, a modified implementation of the above described normal scan flip-flop is proposed where the output Q to a constant logic high (1) value during the scan mode is freezed, and use an alternate output SQ to shift the test vectors serially, which is already available in the circuit. This method uses a performance enhancing circuitry to eliminate the delay overhead caused by the transmission gate blocking logic and also improves the overall performance of the scan flip-flop. Using this scheme, the unnecessary switching in combinational circuit during shift phase of a scan-based test is eliminated, thereby minimising the shift power. The modified transistor level implementation of the scan flip-flop with the blocking logic and performance enhancing circuitry is shown in Figure 3.

The modified scan flip-flop has two outputs, i.e., Q and SQ, the former one goes to combinational circuit and the latter is used for serially shifting test data during test mode. The modified scan cell uses the output Q during functional mode and the output SQ during test mode for serially shifting the scan vectors.

The modified scan cell uses a transmission gate and a pull-down network, shown inside the dotted line (blue coloured) polygon in Figure 3, to freeze the input signal SD1 to a logic '0' value, which in turn set the output Q to a logic '1' value during the entire scan shift operation. The transmission gate and pull down transistor N19 is controlled by the TE (test enable) and TEN (test enable bar) signals. In test mode, the TE signal will be always high (1) and TI is selected in the multiplexer. So, in test mode, when the TE signal is set to 1, the blocking logic transmission gate will be OFF and the pull-down transistor N19 will be ON. This will pull-down the inverter input signal SD1 to 0, which in turn ensures a constant 1 value at output Q during the entire shift operation.

**Figure 3** Proposed scan flip-flop implementation (see online version for colours)




However, the other output signal SQ will follow the test input TI and hence can be used to shift the test vectors. In test mode, it is a general practice in industry to run the circuit at a much lower frequency as compared to functional frequency. Also the SQ output has to drive only the TI input of the successive scan flip-flop in the scan chain. So, output signal SQ can be used to shift in the test data without any timing-related issue. In functional mode TE will be always low (0). When the TE signal is set to 0, the blocking logic transmission gate will be always ON and pull-down transistor N19 will be OFF. The output Q will now follow the functional input D.

The blocking logic transmission gate comes into the functional path which increases functional path delay. For critical paths this delay degrades the overall circuit performance. To overcome this problem a performance enhancing circuitry is used, which not only eliminates the delay penalty caused by blocking logic but also improves the overall performance of the circuit. The performance enhancing circuitry is shown in the dotted dashed line (green coloured) rectangle in Figure 3. This circuitry consists of a TE signal controlled domino style inverter followed by a clock signal controlled transmission gate. The circuit will be active only during functional mode, i.e., when TE is 0 and TEN is 1. The input of this circuit is driven by the signal N1 which is also input to the master latch. So during functional mode the output MD1 of this circuit will be always same as output MD of the master latch because both MD and MD1 will always follow

inverted value of N1. The clock controlled transmission gate opens only during HIGH clock pulse, and eliminates any possibility of fighting between SD1 and MD1 during LOW clock pulse. In other words, it allows the MD1 signal to pass only at the same time when the slave opens. As it can be seen from Figure 3 that the blocking logic transmission gate comes only between SD and SD1 and not coming in between MD1 and SD1. So the MD1 signal assists the SD signal to speed up the switching of the inverter which drives output Q. Hence the performance enhancing circuitry not only eliminates the performance overhead of the blocking logic, but also, improves the overall performance of the scan flip-flop. This method has an additional overhead of six extra transistors, so this approach is better suited to critical paths only and overall area overhead due to extra circuitry used in the scan flip-flop to eliminate delay of the output gating logic will be marginal as the number of critical paths in a circuit is 1–2%. For the rest paths we can use transmission gate-based output gating technique to reduce shift power. Other way to overcome the delay penalty due to TG in normal topology can be solved by over-sizing and reducing the effective resistance or it can be compensated by sizing other transistors but the problem with over sizing is self loading phenomena due to which we cannot increase the size beyond a certain limit. This topology is resilient to self loading phenomena.

## 3 Experimental results

The post layout simulation on ELDO (SPICE tool) using 130 nm technology is carried out at the operating voltage of 3.3 V. Clock to Q delay of the proposed scan flip-flop is compared with the scan flip-flop used in Yang et al. (2008) and the scan flip-flop proposed in Khatri and Ganeshan (2008). The scan flip-flop used in Yang et al. (2008) is a normal scan flip-flop without any output gating logic and the scan flip-flop proposed in Khatri and Ganeshan (2008) uses a transmission gate followed by a pull-up structure for output gating. The layout of scan flip-flop used in Khatri and Ganeshan (2008) and Yang et al. (2008) and the proposed scan flip-flop is drawn in Mentor Graphics IC Studio which uses NMOS to PMOS W/L ratio equal to 2, i.e., $(W/L)p = 2(W/L)n$. The layout of the proposed scan flip-flop is shown in Figure 5. Parasitic were extracted from the layout and simulated the circuit using ELDO SPICE from 100 MHz to 500 MHz clock frequency. The simulation results of the proposed scan flip-flop at clock frequency of 100 MHz have been put for reference in Figure 4.

These results verify the functionality of the proposed design. As shown in Figure 4, when TE signal is set to logic high (1) in test mode, Q get to logic high (1) and does not change throughout the entire scan shift, which maintains the combinational block inputs to a constant logic high (1) value and eliminates the redundant switching in the combinational logic during scan. However, it can also be seen that SQ follows signal TI as long as TE is high (1). When signal TE is set to low (0), both Q and SQ follow D. We have measured clock (CP) to Q propagation delay of slave latch for a constant capacitive load of 0.1 pf, for scan flip-flop in Khatri and Ganeshan (2008) and Yang et al. (2008), and the proposed scan flip-flop.

**Figure 4** Post layout timing results from ELDO at 100 MHz (see online version for colours)

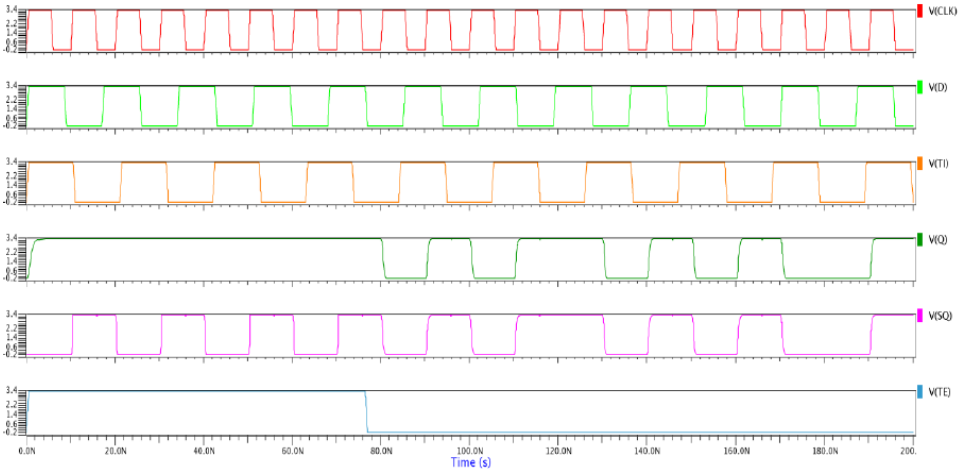
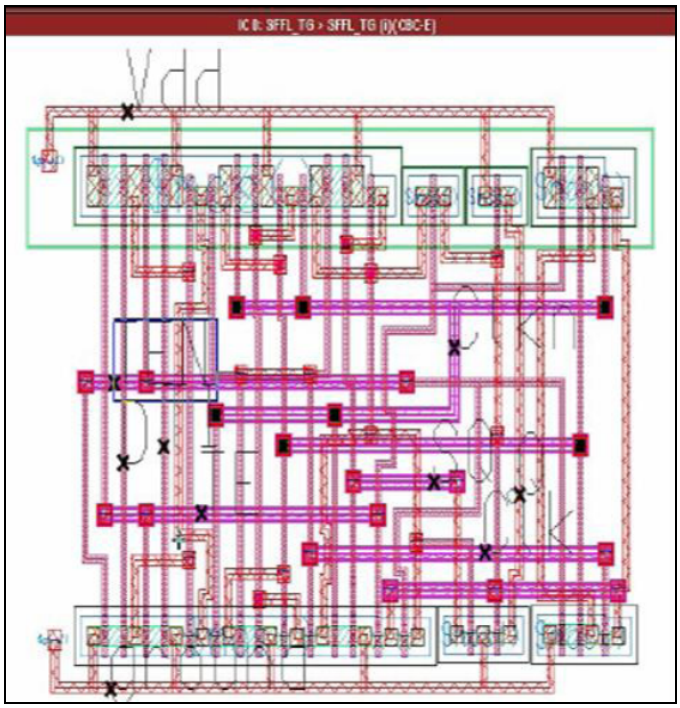



**Figure 5** Layout of the proposed scan flip-flop for critical paths (see online version for colours)




As shown in Table 1, for a fixed capacitive load of 0.1pf, the propagation delay tp of the proposed scan flip-flop's slave latch is found to be 11.50% less than the normal scan flip-flop (Yang et al., 2008), whereas it is 32.84% less than the scan flip-flop in Khatri and Ganeshan (2008) with transmission gate masking technique.

**Table 1** Slave latch clock to Q delay (ps)

| *Capacitive load* | *Considered normal SFF (Yang et al., 2008)* | *Transmission gate masking (Khatri and Ganeshan, 2008)* | *Proposed SFF* | *% improvement w.r.t. (Khatri and Ganeshan, 2008)* | *% improvement w.r.t. (Yang et al., 2008)* |
|---|---|---|---|---|---|
| 0.1 pf | 413.83 | 545.34 | 366.21 | 11.50 | 32.84 |

The main advantage of the proposed scan flip-flop design is that it not only eliminates the performance overhead but also significantly improves the performance as compared to all the earlier reported output gating techniques have severe performance overhead which prohibited their use for timing critical paths. Additionally it eliminates the redundant switching in combinational circuitry during the scanning of test vectors inside a scan chain. If we consider the number of transistor as a rough metric of area estimation, then the proposed scan flip-flop uses six extra transistors as compared to scan flip-flop in Khatri and Ganeshan (2008) and nine extra transistors as compared to normal scan flip-flop (Yang et al., 2008). The large area overhead of the proposed scan flip-flop restricts its use to replace all normal flip-flops in the design. However, as the new scan flip-flop targets only the critical paths, the overall area overhead due to extra circuitry used in the scan flip-flop to eliminate delay of the output gating logic will be marginal as the number of critical paths in a circuit is 1–2% of total number of paths.

## 4 Conclusions and future work

We have proposed a new scan flip-flop design for the critical path which may be used to eliminate the unnecessary power dissipation during serial scan of test vectors. This method uses a performance enhancing circuitry for the elimination of the delay overhead caused due to the transmission gate used as blocking logic and it also improves the overall performance of the scan flip-flop. In conventional scan flip-flop, the combinational circuit has to respond to all the unnecessary transitions thereby dissipating more power. This unnecessary switching can be eliminated using gating methods but it tends to reduce the performance of the circuit. Our design overcomes this problem by using performance enhancing circuitry and this design is better suited for critical paths as it uses six extra transistors compared to the design proposed by Khatri and Ganeshan (2008).

In this work, the experimental results supporting the proposed low power scan techniques are comparing only test case. Power dissipation during the active mode (functional) when there are six additional transistors also needs to be evaluated. In this work, only the test power that is dissipated in the combinational block alone is targeted but in new technology nodes, leakage and clock power are also more critical. Other components, such as internal power (where a cell dissipates power even when its outputs remain stable, because of clocking activity and other input changes) is not affected by the Q-gating at all. Furthermore, the power dissipation of flip-flops itself is usually considered as 30% of the entire power dissipation. So, in new technologies the margin for saving could be very small. In this view, the proposed approaches could be augmented to reduce other power components.

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