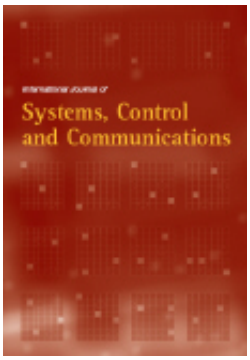


International Journal of Systems, Control and Communications

ISSN online: 1755-9359 - ISSN print: 1755-9340
https://www.inderscience.com/ijscc

A soft processor MicroBlaze-based adaptive power line interference canceller for biomedical signal processing

Abhay Kasetwar, Sanjay Gulhane, Vicky Butram

DOI: 10.1504/IJSCC.2025.10069428

Article History:

Received:	22 May 2023
Last revised:	20 July 2023
Accepted:	04 November 2024
Published online:	18 February 2025

A soft processor MicroBlaze-based adaptive power line interference canceller for biomedical signal processing

Abhay Kasetwar

Department of Electronics and Telecommunication,
S.B Jain Institute of Technology, Management and Research,
Nagpur, Maharashtra, India
Email: abhaykasetwar@gmail.com

Sanjay Gulhane

Department of Electronics and Telecommunication,
Pravara Rural Engineering College,
Loni, Ahmednagar, India
Email: sanjay.gulhane@pravara.in

Vicky Butram*

Department of Electronics,
Ramdeobaba University,
Nagpur, Maharashtra, India
Email: butramv1@rknec.edu
*Corresponding author

Abstract: In this work, two different adaptive algorithms for PLI removal; PID-based response adjustment for reducing error (PID-RARE) and PID-based coefficient adjustment for reducing error (PID-CARE) proposed in the literature are tested for their hardware compatibility and accuracy. FPGA-based biomedical signal processing systems have great computational speed and low power consumption, but typical HDL programming is time-consuming. New high-level programming tools for FPGA design, including SOC solutions, make development easier while retaining performance. The MicroBlaze is considered as innovative platform for developing an adaptive power line interference canceller. Here PID-CARE and PID-RARE algorithms are implemented on FPGA using soft-core processor based on MicroBlaze platform. The performances of the implemented algorithms are evaluated on the basis of output signal to noise ratio (SNRout), correlation coefficient (CC), mean square error (MSE) and percent root mean square difference (PRD). Finally hardware and software results are compared for justifying hardware compatibility and accuracy.

Keywords: power line interference; PLI; adaptive algorithm; PID; NSLMS; PID-based response adjustment for reducing error; PID-RARE; PID-based coefficient adjustment for reducing error; PID-CARE; MicroBlaze; field programmable gate array; FPGA.

Reference to this paper should be made as follows: Kasetwar, A., Gulhane, S. and Butram, V. (2025) 'A soft processor MicroBlaze-based adaptive power line interference canceller for biomedical signal processing', *Int. J. Systems, Control and Communications*, Vol. 16, No. 1, pp.33–44.

Biographical notes: Abhay Kasetwar did his MTech in Electronics Engineering and PhD in Electronics Engineering with specialisation in adaptive signal processing from RTM Nagpur University, Nagpur. He has a total 15 years of teaching experience and is currently working as professor, S.B. Jain Institute of Technology, Management and Research, Nagpur. He has a total 25+ publications in reputed journals and conferences. He is guiding four research scholars in various domain of electronic engineering.

Sanjay Gulhane did his BE in Electronics Engineering, MTech (Telecommunication Systems Engineering) and PhD (Communication Engineering), all from IIT Kharagpur. He has a total 34 years of teaching experience and currently working as a Principal, Pravara Rural Engineering College, Loni, Ahmednagar. He has to his credit publication of 50 plus papers in national/international journals/conferences proceedings. He is a Governing Council member of IETE and member of IEI and ISTE.

Vicky Butram received his PhD in Electronics and Communication Department from National Institute of Technology, Raipur, India and Master's degree in VLSI Design from Shri Ramdeobaba College of Engineering and Management, Nagpur, India. He served as a Senior Research Fellow under (Department of Science and Technology) DST-SERB project with the Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology Design and Manufacturing in. Currently, He is working as an Assistant Professor in the Department of Electronics in Ramdeobaba University, Nagpur, India.

1 Introduction

Biomedical signal processing is currently one of the most popular study areas. The biomedical signals contain significant information about the patient's health in very fine aspects. Consequently, noise-free biological signals are required for accurate diagnosis. Biomedical signals like electrocardiogram (ECG), electroencephalogram (EEG), and electromyography (EMG), etc. are badly affected by non-stationary interferences. So, it is difficult to get accurate results for such biomedical signal recordings. Power line interference (PLI) is a dominant one that disturbs the spectrum of required biomedical signals (Ziarani and Konrad, 2002; Surekha and Patil, 2021; Mihov, 2013). As per the American Heart Association recommendation, biomedical signal recorders have a 3 dB range of frequencies from 0.67 Hz to 150 Hz (Razzaq et al., 2016). The captured biomedical signals are distorted by power line interference because the power line frequency is within the range of biomedical signals. The interest signal and the additional interference make up the corrupted signal that is measured (Malghan and Hota, 2023; Goldberger et al., 2000). An optimal solution for power line interference reduction should get rid of the interference while keeping the signal intact. For this, the two main methods viz notch filter and adaptive interference canceller are proposed in Ider and Koymen (1990).

The PLI is successfully eliminated by the narrow suppression band filters. The notch filter's suppression band should be as narrow as feasible. If the frequency of power line interference is precisely 50 Hz or 60 Hz, a sharp notch filter can decrease interfering noise. When the power line frequency is unstable or improperly set, problems start to occur. A mismatch between the suppression band and the power line frequency might result in insufficient power line interference (PLI) reduction. An increase in the stop-band width of the notch filter may remove the PLI effectively and make the filter design simple however; larger stop-band width affects the characteristics of the clean signal. Therefore the use of a simple notch filter cannot remove the non-stationary PLI in the signal (Avendaño-Valencia et al., 2007).

One method for considering frequency fluctuations is the application of an adaptive notch filter. A filter that automatically modifies its coefficients in response to changes in the parameters of the interference noise is known as an adaptive filter (Zhang et al., 2010; Boroujeny, 2013). The most common tools for the real-time implementation of adaptive filtering applications are application-specific integrated circuits (ASIC), digital signal processor (DSP), and field programmable gate array (FPGA). DSPs are used for extremely complex math-intensive tasks, but their serial architecture prevents them from processing high sampling rate applications. The ASIC lacks flexibility and necessitates a lengthy design cycle. The FPGA can compensate for the shortcomings of ASIC and DSP (Bahoura and Ezzaidi, 2009).

Adaptive cancellers may be implemented using FPGA, and this offers several benefits. FPGAs make it possible to adjust the canceller and shorten design time. Concurrent programming algorithms enable parallel signal processing with multiple input ECG signals on a single FPGA without sacrificing speed (Ramos et al., 2007). Most biomedical signal processing devices demand high computing capability while consuming less power; FPGA addresses both of these criteria. As a result, developing a biological signal processing system using FPGA is acceptable (Ramos et al., 2007).

2 Related work

The most popular approach for repeatedly reducing the mean square error (MSE) of the system output is the least mean square (LMS). Attempts are made to implement the LMS algorithm in FPGA utilising the model-based design new development approach (Zhou et al., 2011). Bahoura and Ezzaidi (2011) have implemented the adaptive noise canceller using sequential, parallel, and pipelined architectures on FPGA boards using Xilinx System generator flow. It is observed that the sequential system required fewer resources as compared to the parallel architecture along with providing comparable filtering performance.

When compared to the regular LMS method, the convergence behaviour of the delayed least mean squares (DLMS) algorithm degrades and worsens as the adaption delay increases (Ramanathan and Visvanathan, 1996). Ramos et al. (2001) developed an adaptive canceller for 50 Hz interference in electrocardiography applications utilising programmable logic devices of the FPGA type and the LMS adaptive algorithm. Because it is resistant to changes in the interference signal, the technique outperforms standard solutions. The modified Faddeev's method and one trapezoidal array are used to illustrate an efficient systolic implementation of the Kalman filtering issue (Chen and Guo, 2005).

Tomasini et al. (2016) demonstrated the implementation of an adaptive power line filter based on the RLS (APF-RLS) method using an embedded system platform. This approach provides the highest performance in terms of output SNR and best retains the frequency characteristics of the targeted signals while requiring the least amount of processing. Bahoura and Ezzaidi (2010) used Xilinx System Generator for DSP to construct a wavelet-based denoising technique using FPGA to eliminate PLI from the ECG signal. It is a high-level software tool that allows you to generate and test hardware designs for Xilinx FPGAs using the MATLAB/Simulink environment. In Jindapetch et al. (2012), the authors provide surface electromyography (sEMG) FPGA implementations of an adaptive filter for power-line noise reduction based on an adaptive linear neural network (ADALINE). The 16-bit fixed-point Q 0.15 format ADALINE filter was determined to be appropriate for implementation due to its small circuit size.

The MicroBlaze embedded processor softcore is a reduced instruction set computer (RISC) that has been designed for use in Xilinx FPGAs. The MicroBlaze platform offers a highly customisable architecture while offering the essential processing system with the fewest system resources feasible (Suhasini et al., 2014). Xilinx's Embedded Development Kit (EDK) software suite contains the MicroBlaze together with a standard set of peripherals. The EDK kit includes a complete set of GNU-based software tools, including a compiler, assembler, debugger, and linker, as well as support for many Xilinx FPGA families, notably the Spartan-3 series (Rosinger, 2004). In Choo and Mutsuddy, (2006), the authors created an embedded-based NLMS adaptive filter system using a flexible LMS core and a Xilinx MicroBlaze soft processor, both of which are implemented on a Xilinx Spartan-3 FPGA. Thus, the resulting architecture is referred to be an embedded DSP system, which is especially beneficial for adaptive FIR filters with parameterisable data bit width and tap length. Two architectures for real-time adaptive noise cancelling based on the MicroBlaze soft processor and implemented on FPGA were recently reported in Bahoura and Ezzaidi (2015). The first design employs the least mean square (LMS) method, while the second employs a scaled variant of the normalised least mean square (NLMS) technique. In Mimouni and Karim (2013), the authors built and constructed a soft processor MicroBlaze-based embedded system for cardiac monitoring. It was created using the EDK suite tools and C code in the Xilinx kernel RTOS environment. In Elhossini et al. (2006), three distinct designs on FPGA are used to implement the LMS algorithm. The method is used to a voice signal to improve its signal-to-noise ratio (SNR). The three designs are intended for audio processing, and they make use of the Xilinx multimedia board and the MB softcore.

From the literature survey, it can be concluded that, since FPGA is programmed by hardware description language (HDL), the implementation using FPGA achieves a high speed of operation. However, programming FPGAs in HDL takes too long and requires knowledge of chip design (Sugadev et al., 2022). This scenario has changed during the last decade as a new class of high-level programming tools and languages for FPGA design has emerged. In system-on-a-chip (SOC) solutions, FPGAs may merge customised user cores with a soft or hard-embedded CPU. The MicroBlaze is one of the advanced platforms for developing the adaptive power line interference canceller which can be used as the customised core for implementation on FPGA. The MicroBlaze platform helps in reducing the resource utilisation for hardware realisation on FPGA.

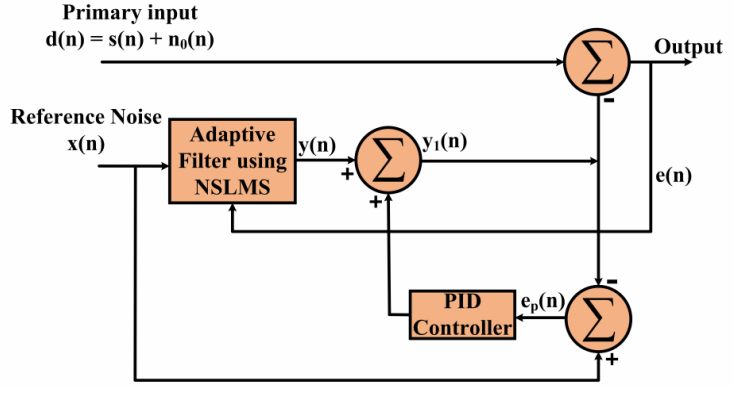
3 Adaptive power line interference canceller

This section gives a brief overview of two methods of adaptive PLI cancellation already proposed in the literature named proportional integral derivative-based response adjustment for reducing error (PID-RARE) and proportional integral derivative-based coefficient adjustment for reducing error (PID-CARE) in Subsections 3.1 and 3.2 (Kasetwar and Gulhane, 2017). Further in Section 3.3, the authors have realised both the algorithms on FPGA using the MicroBlaze platform for checking their hardware compatibility.

3.1 PID-based response adjustment for reducing error

The block diagram of PID-RARE is shown in Figure 1. The target of the adaptive algorithm is to minimise the difference between the adaptive filter output $y(n)$ and interfered signal $n_0(n)$ thereby making $y(n)$ close to $n_0(n)$.

Figure 1 Adaptive PLI canceller using PID–RARE algorithm (see online version for colours)



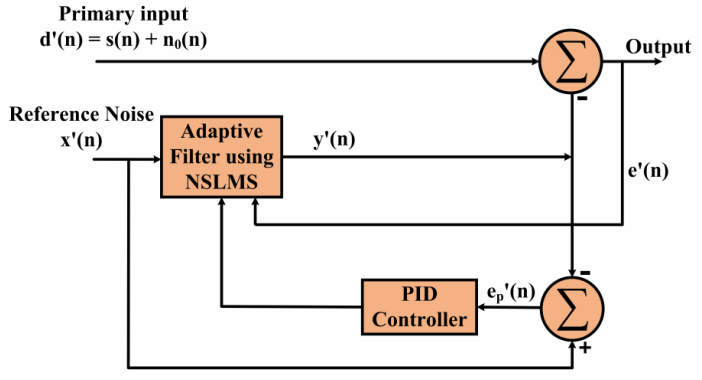
The adaptive filter output is then subtracted from noisy data $d(n)$ to get a clean ECG signal $e(n)$ at the output. In the PID-RARE algorithm, the PID is used to correct the adaptive filter response $y(n)$ to $y_1(n)$. The input to the PID is the difference between the corrected response $y_1(n)$ and the reference noise $x(n)$. The function of PID is to make the output of NSLMS $y(n)$ which is generated from reference noise $x(n)$, close to $n_0(n)$.

The PID loop updates the $y(n)$ to $y_1(n)$ which is closer to $n_0(n)$. In this algorithm, for every input window sample, the PID runs multiple times till it achieves the minimum error value ε at its input. The corrected output $y_1(n)$ is then subtracted from the input noisy signal $d(n)$ to get the error signal $e(n)$. This error signal $e(n)$ is feedback to NSLMS and is used for the updation of filter coefficients to provide corrected filter output y1(n) close to $n_0(n)$. In every iteration of NSLMS, the use of PID aids in obtaining more optimal values of filter coefficients which helps the NSLMS algorithm to converge in a lesser amount of time thereby improving its performance.

3.2 PID-based coefficient adjustment for reducing error

The block diagram of PID-CARE is shown in Figure 2. In adaptive filtering, an error between the adaptive filter output $y(n)$ and interfered signal $n_0(n)$ is minimised which can be achieved by adjusting the filter coefficients w to optimal values iteratively.

Figure 2 Adaptive PLI canceller using PID-CARE algorithm (see online version for colours)



The weight updation process decides the rate of convergence as well as the performance of an algorithm. The operation of PID-CARE differs from that of PID-RARE in the sense that in PID-RARE, the PID is used to update the filter response and thereby update the filter coefficients whereas in PID-CARE, the PID output is directly used to update the filter coefficients and thereby updating the filter response.

In PID-RARE, the PID is used to update the filter response and thereby updating the filter coefficients whereas in PID-CARE, the PID output is directly used to update the filter coefficients and thereby updating the filter response. Moreover, the PID runs multiple times during each iteration of NSLMS algorithm in PID-CARE. In every iteration of NSLMS, the more optimal values of filter coefficients are obtained by the use of PID which helps the NSLMS algorithm to converge in lesser amount of time and thereby improving the performance.

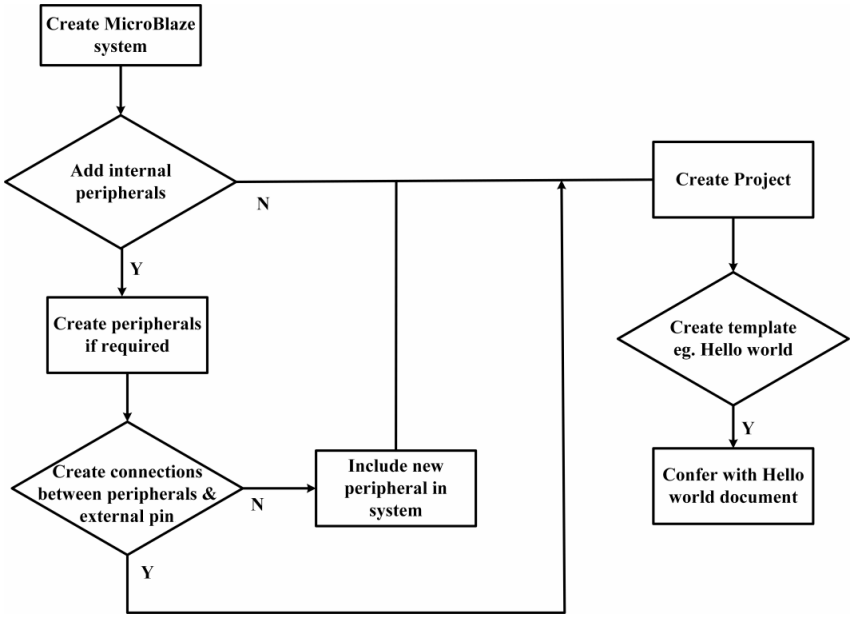
3.3 Hardware realisation of PID-RARE and PID-CARE on FPGA using MicroBlaze

Xilinx EDK, a suite of tools and intellectual property (IP) that allows the creation of a fully embedded processor system for implementation in a Xilinx FPGA, was employed as a development tool in our work. Xilinx Platform Studio (XPS) and the software development package (SDK) are included in the whole package:

1 The development environment for creating the hardware portion of an embedded processor system is XPS. On the NEXYS-3 device, it is utilised to generate the MicroBlaze system. It enables hardware designers to quickly create, connect, and configure embedded processor-based systems.

2 In addition to XPS, the software development kit (SDK) offers a complete development environment for the development and verification of C/C++ embedded software applications (Mimouni and Karim, 2013).

Figure 3 MicroBlaze process flowchart



Once the MicroBlaze system has been created in XPS, the application C program can be written using the SDK. The work also requires the use of Digilent Adept software for programming the NEXYS 3. As a development board, we have used the Nexys 2-500 of Digilent that features Xilinx's Spartan-3 series FPGA.

3.3.1 Process flowchart

Figure 3 shows the process flowchart describing the process for creating any application using MicroBlaze. The process flow was initiated by creating a MicroBlaze system using XPS. There is a provision for adding an internal peripheral or creating a new peripheral as per the requirement of a particular application. Peripheral creation is followed by the creation of connections between peripherals and external pins. In the next step, C/C++ embedded software application creation and verification is performed using SDK. The stepwise flow to build and run the proposed systems on the MicroBlaze platform for their implementation on FPGA is discussed in Section 3.3.2 (Elhossini et al., 2006).

3.3.2 Building of the systems using XPS and SDK

Designing the system using MicroBlaze starts with developing a repository created on the hard disc to store the customised IP core. This repository folder needs to have three subfolders; Plan_Ahead, SDK_Project, and XPS_Project. This folder also contains the Nexys-3 Board support files for the EDK BSB wizard which is downloaded from the

Digilent website. XPS environment is used to create a new MicroBlaze system in the internal architecture of FPGA supported with a base system builder file in the repository. A single processor system with 50 MHz clock frequency and 32 KB memory on 'Nexys2-500' board with PLB system to communicate with the other peripherals is used.

The C/C++ application code for the proposed systems is written in SDK wizard. After writing and saving the required application, the code is auto build and ready for programming in FPGA. The Nexys 2-500 SPARTAN-3 Development Board is programmed with the developed C/C++ application code. The snapshot of the real time execution of proposed systems on Nexys 2-500 SPARTAN 3 Development Board is shown in Fig. 4.

4 Results

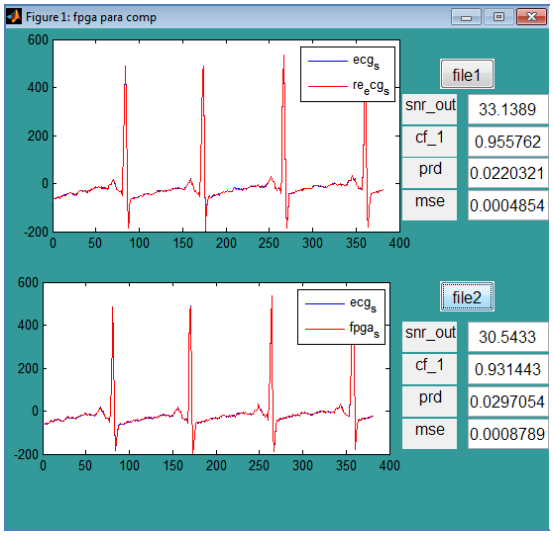
The results obtained from the FPGA implementation of PID-RARE and PID-CARE algorithms are fetched using serial port. The sample values of filtered output are plotted and all the evaluation parameters are determined in MATLAB environment.

Figure 4 Real time execution of adaptive noise canceller on Nexys 2-500 SPARTAN 3 Development Board (see online version for colours)

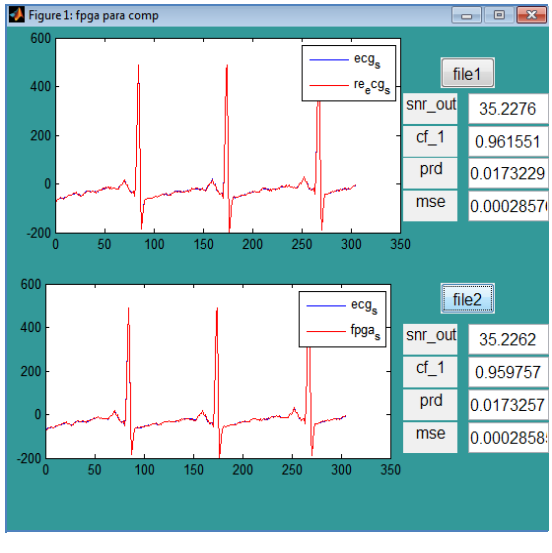
Figure 5(a) shows the comparison of performance evaluation parameters obtained from the simulated system in MATLAB and those obtained from hardware implementation using MicroBlaze for PID-RARE. The SNR_{in} equals to 0 dB is considered. The upper half part of the figure represents the time domain waveforms obtained from the simulated system in MATLAB by processing through PID-RARE algorithm. The right part of the upper half of the figure indicates the values of SNR_{out} in dB, CC, PRD and MSE for PID-RARE simulated in MATLAB. The lower half part of the figure represents the results of PID-RARE obtained from its hardware implementation in FPGA using MicroBlaze. The overlapping of the output waveforms represented by red colour with the clean ECG signal represented by blue colour indicates the ability of PID-RARE to

provide output waveforms closer to the clean signal. The values of SNR_{out}, CC, PRD and MSE obtained from the MATLAB simulated PID-RARE are 33.1389 dB, 0.9558, 0.0220 and 0.0004854 respectively whereas these values obtained from the hardware implementation are 30.54 dB, 0.9314, 0.0297 and 0.0008789 respectively. The closer of the time domain waveforms and the values of the performance evaluation parameters prove the correctness of hardware realisation of PID-RARE in FPGA using MicroBlaze.

Figure 5 Comparison of results of (a) PID-RARE and (b) PID-CARE simulated in MATLAB and for its hardware implementation at SNRin = 0 dB (see online version for colours)



(a)



(b)

Table 1 Comparison of simulation and hardware result for PID-RARE and PID-CARE

Evaluation parameter	*PID-RARE*		*PID-CARE*	
	Simulation result	*Hardware result*	*Simulation result*	*Hardware result*
Output signal to noise ratio (SNR_{out})	33.1398	30.5433	35.2276	35.2262
Correlation coefficient (CC)	0.9557	0.9314	0.9615	0.9597
Percent root mean square difference (PRD)	0.0220	0.0297	0.01732	0.01732
Mean square error (MSE)	0.00048	0.00087	0.00028	0.00028

Figure 5(b) shows the performance comparison obtained from PID-CARE simulated in MATLAB and those obtained from its hardware implementation using MicroBlaze at SNR_{in} equal to 0 dB. The time domain waveforms for clean ECG signal and the signal obtained after processing through PID-CARE in MATLAB simulator are shown in the upper half part of the figure. It also depicts the values for different performance evaluation parameters for PID-CARE. The lower half part of the figure represents the results obtained after processing through PID-CARE obtained from its hardware implementation in FPGA using MicroBlaze.

The overlapping of output waveforms with clean ECG signal waveforms indicates the ability of PID-CARE to provide output waveforms closer to the clean signal. Further, it can be observed that the output waveform of PID-CARE more closely overlaps the clean ECG signal than that in PID-RARE. The values of SNR_{out}, CC, PRD, and MSE obtained from the PID-CARE simulated in MATLAB are 35.2276 dB, 0.9615, 0.0173, and 0.0002857 respectively whereas these values obtained from the hardware implementation are 35.2262 dB, 0.9597, 0.0173 and 0.0002858 respectively. From Table 1, it is found that the highly closer values of performance metrics for PID-CARE obtained from the simulated system and its hardware implementation indicate that PID-CARE is more hardware compatible than PID-RARE.

5 Conclusions

This work investigates the applicability of the PID-RARE and PID-CARE algorithms for their real time implementation. The realisation of these algorithms using MicroBlaze platform is carried out. The results obtained from the hardware realisation are used for their comparative performance analysis with those obtained from software implementation of the algorithms in order to justify the compatibility and accuracy at hardware level. The closer values of the obtained results from hardware implementation to those obtained from software implementation prove the hardware compatibility of both the algorithms.

References

Avendaño-Valencia, L.D., Avenda, L.E., Ferrero, J.M. and Castellanos, G. (2007) 'Improvement of an extended kalman filter power line interference suppressor for ECG signals', in *Computer in Cardiology*, November, Vol. 34, pp.553–556.

Bahoura, M. and Ezzaidi, H. (2009) 'FPGA-implementation of a sequential adaptive noise canceller using Xilinx system generator', *Int. Conf. on Microelectronics*, December, Marrakech, Morocco, pp.213–216.

Bahoura, M. and Ezzaidi, H. (2010) 'FPGA-implementation of wavelet-based denoising technique to remove power-line interference from ECG signal', *Proc. Int. Conf. on Info. Tech. and Appli. in Biomed. (ITAB)*, November, Corfu, Greece.

Bahoura, M. and Ezzaidi, H. (2011) 'FPGA implementation of parallel and sequential architectures for adaptive noise cancellation', *Circuit Sys. and Sig. Proc.*, December, Vol. 30, No. 6, pp.1521–1548.

Bahoura, M. and Ezzaidi, H. (2015) 'Real-time implementation of an adaptive noise canceller based on MicroBlaze soft processor', *IEEE 28th Canadian Conference on Electrical and Computer Engineering*, May, Halifax, Canada, pp.1180–1183.

Boroujeny, B.F. (2013) *Adaptive Filters: Theory and Applications*, May, Wiley, ISBN: 978-1-119-97954-8.

Chen, G. and Guo, L. (2005) 'The FPGA implementation of Kalman filter', *Proc. Int. Conf. on Sig. Proc., Comp. Geo. and Artif. Vision*, September, Malta, pp.61–65.

Choo, C. and Mutsuddy, S. (2006). An embedded adaptive filtering system on fpga. Department of Electrical Engineering, San Jose State University, San Jose, CA, 95198-0084.

Elhossini, A., Areibi, S. and Dony, R. (2006) 'An FPGA implementation of the LMS adaptive filter for audio processing', *Int. Conf. on Reconfig. Comp. and FPGA's*, September, San Luis Potosi, Mexico.

Goldberger, A., Amaral, L., Glass, L., Hausdorff, J., Ivanov, P.C., Mark, R. and Stanley, H.E. (2000) 'PhysioBank, PhysioToolkit, and PhysioNet: components of a new research resource for complex physiologic signals', *Circulation*, Vol. 101, No. 23, pp.e215–e220.

Ider, Y.Z. and Koymen, H. (1990) 'A new technique for line interference monitoring and reduction in biopotential amplifiers', *IEEE Trans. on Biomed. Eng.*, June, Vol. 37, No. 6, pp.624–631.

Jindapetch, N., Chewae, S. and Phukpattaranont, P. (2012) 'FPGA implementations of an ADALINE adaptive filter for powerline noise cancellation in surface electromyography signals', *Measurement*, April, Vol. 45, No. 3, pp.405–414.

Kasetwar, A. and Gulhane, S. (2017) *Adaptive Filtering for Power Line Interference Canceller*, Application Number: 201721006414A, 3 October.

Malghan, P.G. and Hota, M.K. (2023) 'An improved VME technique via heap based optimization algorithm and AWIT method for PLI and MA noise elimination in ECG', *IEEE Access*, Vol. 11, pp.54070–54079.

Mihov, G. (2013) 'Complex filters for the subtraction procedure for power-line interference removal from ECG', *International Journal of Reasoning-based Intelligent Systems*, Vol. 5, No. 3, pp.146–153.

Mimouni, H. and Karim, M. (2013) 'A soft processor MicroBlaze-based embedded system for cardiac monitoring', *Int. Jour. of Adv. Comp. Sci. and Appl.*, Vol. 4, No. 9, pp.48–53.

Ramanathan, S. and Visvanathan, V. (1996) 'A systolic architecture for LMS adaptive filtering with minimal adaption delay', *Proc. Int. Confe. on VLSI Des.*, January, Banglore, India, pp.286–289.

Ramos, R., Lazaro, A.M., Del Rio, J. and Olivar, G. (2007) 'FPGA-based implementation of an adaptive canceller for 50/60-Hz interference in electrocardiography', *IEEE Trans. on Instr. and Meas.*, December, Vol. 56, No. 6, pp.2633–2640.

Ramos, R., Manuel, A., Olivar, G., Trullols, E. and Del Rio, J. (2001) 'Application by means of FPGA of an adaptive canceller 50 Hz interference in electrocardiography', *Int. Conf. on Instr. and Meas. Tech.*, May, Budapest, Hungary, pp.32–37.

Razzaq, N., Sheikh, S.A.A., Salman, M. and Zaidi, T. (2016) 'An intelligent adaptive filter for elimination of power line interference from high resolution electrocardiogram', *IEEE Access*, Vol. 4, pp.1676–1688.

Rosinger, H-P. (2004) 'Connecting customized IP to the MicroBlaze soft processor using the fast simplex link (FSL) channel', *XAPP529*, May, Vol. 1.3.

Sugadev, M., Kaushik, M., Vijayakumar, V. and Ilayaraaja, K.T. (2022) 'Performance analysis of adaptive filter algorithms on different noise sources', *2022 International Conference on Computer Communication and Informatics (ICCCI)*, January, IEEE, pp.1–5.

Suhasini, V.K., Sekhar, K.N.C. and Reddy, R.M. (2014) 'Design and implementation of adaptive filtering algorithm for noise cancellation in speech signal on FPGA', *Int. Jour. of Scientific Eng. and Tech. Res.*, November, Vol. 03, No. 41, pp.8390–8396.

Surekha, K.S. and Patil, B.P. (2021) 'Power line interference removal from electrocardiogram signal using multi-order adaptive LMS filtering', *International Journal of Biomedical Engineering and Technology*, Vol. 35, No. 2, pp.135–151.

Tomasini, M., Benatti, S., Milosevic, B., Farella, E. and Benini, L. (2016) 'Power line interference removal for high quality continuous bio-signal monitoring with low-power wearable devices', *IEEE Sensors Journal*, May, Vol. 16, No. 10, pp.3887–3895.

Zhang, W.W., Li, M. and Zhao, J.Y. (2010) 'Research on ECG signal noise reduction based on wavelet multi-resolution analysis', *Proc. of the Int. Conf. on Wavelet Analysis and Pattern Recognition*, September, Qingdao, China, pp.351–354.

Zhou, Z., He, J. and Liu, Z. (2011) 'FPGA-implementation of LMS adaptive noise canceller for ECG signal using model based design', *IEEE International Sym. on Bioelectr. and Bioinfo.*, December, Suzhou, China, pp.127–130.

Ziarani, A.K. and Konrad, A. (2002) 'A nonlinear adaptive method of elimination of power line interference in ECG signals', *IEEE Transaction on Biomedical Engineering*, June, Vol. 49, No. 6, pp.540–547.