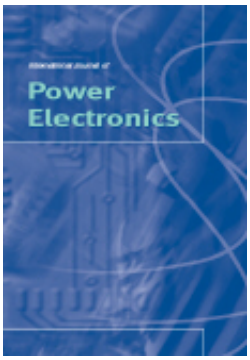

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BLDC drive commutation current ripple minimisation using a high-performance novel active switched inductor and switched capacitor-based QZS DC-DC converter

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Abstract: Although brushless direct current motor (BLDCM) drives are gaining popularity in commercial and industrial applications, a few significant problems and research subjects still have not been conquered and need to be addressed. Its low inductance and electronic commutation both contribute to a decrease in the predicted performance of the motor. The commutation of the phases is the basic cause of the ripples that are present in the form of the current wave. This study introduces a novel approach that utilises a high boost non-isolated quasi-Z-source (qZS) DC-DC converter at the beginning of a BLDC drive, together with an active switched-inductor (ASI) along with a switched-capacitor (SC) and DC link voltage (DCLV) circuit. Using a high step-up non-isolated quasi-Z-source DC-DC converter with ASI and SC, combined with the three-phase voltage source inverter, has effectively minimised the fluctuation in the commutation torque. The control method and switch selector circuit have been incorporated into the system to achieve the desired input DC during the commutation phase. For developing and testing the suggested 325 W drive, MATLAB/Simulink software is utilised. The simulation results demonstrate that the proposed module reduces torque ripples in the commutation region by 40.6% compared to conventional techniques. This illustrates the efficacy of the proposed system.

Keywords: BLDC motor; commutation torque ripple; commutation current ripple; quasi-Z-source; qZS; high gain DC-DC converter; switched capacitor; SC; active switched inductor; ASL.

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1 Introduction

Brushless DC (BLDC) motors are frequently preferred for dynamic applications due to their numerous advantages: high power density, high dynamic responsiveness, high dependability, compact size, and straightforward control. It has many uses in industries such as aviation, vehicles, medical equipment, and home appliances. By 2030, it is expected that BLDC motors will have overtaken traditional induction motors as the prevailing method of power transmission in the industrial sector. BLDC motors will be expected to have a substantial impact in the future due to the estimated rise in demand for electric vehicles in the next decade (Mohanraj et al., 2022b; Prabhu et al., 2023). The worldwide market for brushless DC (BLDC) motors is projected to experience substantial growth, with an estimated valuation of 15.2 billion USD by 2025 (Mohanraj et al., 2022a). Electronically commutated BLDCMs are stable and need less maintenance because they do not have parts that wear out quickly, like a normal mechanical commutator and brush assembly. Nevertheless, in applications that need high levels of accuracy, the issue of torque ripple in BLDCM has consistently been a major constraint on their performance. Excessive torque pulsation can raise motor energy consumption and have an adverse effect on the stability of load output and speed (Viswanathan and Seenithangom, 2018).

In recent decades, there has been considerable interest in studying the reduction of commutation torque ripple because the inherent properties of the structure and the selected control technique can lead to mechanical oscillation and sound generation caused by the fluctuation in torque during commutation (Park et al., 2021). At high speeds, the maximum fluctuation in torque can be as large as 50% of the average torque, which limits the uses of it in industrial applications (Iepure et al., 2012). One can make topological modifications or tweaks to the drive control scheme to mitigate torque ripples. There are three main types of control methods based on the control variables. One approach involves utilising current control. By controlling the pulse width, the torque ripple can be effectively minimised in this approach. The second method makes use of torque as the variable for control. Changing the DC-bus voltage while the commutation takes place is another option. The DC-bus voltage and commutation torque ripple may be achieved with the help of various DC/DC converters (Yao et al., 2019). An incremental predictive control strategy based on unipolar pulse width modulation (PWM) is employed to double the current ripple frequency, thereby reducing the current ripple in the non-commutation interval (Zeng et al., 2024).

Use of the best possible state for switch compensation and duty cycle is done using finite control model predictive control method (FCS-MPC) which helps reduce the computational load by 24.27% compared to the conventional method and switching

frequency (Li et al., 2024). An alternate conduction control approach between the 2-phase and 3-phase conduction modes is suggested in Hassan et al. (2023) and Li et al. (2020). The standard 2-phase conduction mode is chosen during the non-commutation state and an alternative conduction mode (for both 2-phase and 3-phase operation) is employed to minimise the commutation torque ripple during the commutation. By combining an artificial neural network (ANN)-fuzzy self-learning algorithm with real-time rules and numerical data, the SM controller can effectively modulate motor torque with little ripple by anticipating and mitigating error rates in the BLDC motor (Prabhu et al., 2024). An enhanced jellyfish search (ImpJS), improved tunicate swarm optimisation algorithm (ITSA) and the ANFIS-EHO hybrid algorithm method to minimise torque ripple using modified DC-DC converter for a BLDC motor is used for reducing torque ripple over wide range of speed (Rajesh and Saravanan, 2023; Kommula and Kota, 2022; Dasari et al., 2023). The direct torque control-based direct DC-link current control (DDLCC) method is used for rapid and dynamic torque response, offering simple derivative-based method to eliminate ripples in torque while maintaining the absence of its DC offset (Heidari and Ahn, 2024). The implementation of a front-end DC converter in a PAM-BLDC drive results in an improvement of around 40% in torque ripple by using high-bandwidth modulation of the DC-link voltage and current (Huang et al., 2022). The reduction of about 27.6 in commutation torque ripples can be achieved using PWM time delay in the commutation and conduction region (Lee et al., 2023). The supervisory self-learning-based energy management controller improves the efficiency of the BLDC motor by reducing variations in speed, torque, and current. It does this by capturing the nonlinear attributes of the motor's functioning and making appropriate adjustments, resulting in decreased fluctuations in speed and torque inaccuracies under various circumstances (Saiteja and Ashok, 2024).

Hysteresis current control (HMC)-based Z source inverter is used in BLDCC motor to obtain quicker torque response and reduce torque ripple (Dutta et al., 2022). A uniform switching logic has been developed for Hall sensor-controlled BLDCM drives using the maximum torque per ampere (MTPA) control to maintain alignment between the fundamental component of the back EMF and the phase current. This feature enables the motor to go beyond the standard 120° operation, independent of the motor parameters, even if the conduction angle exceeds 120° (Zhou et al., 2023). A new multi-level voltage space vector structure-based control scheme for dual inverter-fed open-end winding BLDC (OEW-BLDC) motor drives with peak current control reduces torque ripple by reducing error voltage vectors while implementing the PWM scheme (Krishna and Rajeevan, 2024). A novel hybrid Y-source-quasi-Z source (YSQZS) DC-DC converter has been developed by combining the benefits of YS and QZS topology to obtain a larger voltage gain and efficiency with fewer components as compared to other Z-source converters (Li et al., 2023). A converter based on QZS topology can be employed for applications requiring high voltage gain, without requiring high duty and turns ratios in the transformer. Operating at a lower voltage and current rating, this architecture allows for the use of MOSFETs due to their ability to handle low voltage requirements and the flexibility to incorporate multiple legs at the input stage (Nafari and Beiranvand, 2023).

Topological modification of the BLDC drive is one of the techniques that is being investigated. During the commutation period, a DC-DC converter is utilised in these topologies to establish the rise time of the incoming phase current. This is accomplished by providing the necessary DC link voltage to VSI. The rapid change of input voltage across the DC link can be achieved by the existence of an auxiliary switch that links the

DC link and the output of the DC-DC converter (Xu et al., 2016; Cao et al., 2019; Li et al., 2016).

A new topology with a Ćuk converter is used to operate BLDC drive in two distinct modes. During the commutation period, it functions as a boost converter, and during the normal conduction phase, it operates as a buck-boost converter. An additional switch that relies on the feedback signal from the Hall sensor is used to minimise fluctuations in torque (Chen et al., 2017). A SICQZS converter with 94.8% efficiency at 500 W output power reduces the inductor core saturation problem and provides high gain at a low duty cycle is proposed in Gopinathan et al. (2023). The hybrid split-inductor-based SEPIC high-voltage gain converter provides more voltage gain, less switching losses and stress, it reduces current ripple by 50% compared to the m-SEPIC converter (Kumar et al., 2022b). Power factor correction (PFC)-based modified zeta converter topology has achieved the best power factor, which is 0.981 (Bin et al., 2023); the relevance of the suggested model for usage in applications that need low power and low cost, since the total harmonic distortion (THD) is the lowest of all three topologies, coming in at 9.81%. About 14.6% of the current ripples and 8.6% of the torque ripples that correspond to them are provided by the model antiseptic control technique. A reduction of 31.7% in current ripples and 32.5% in torque ripples is possible with the utilisation of the PWM-MAC approach (Kumar et al., 2022a). A novel hybrid Ćuk DC-DC converter circuit topology with a high-voltage gain is developed to reduce ripple (Raj et al., 2022). It needs smaller magnetic element sizes, lowering the drive system's weight. Additionally, the larger boosting ratio reduces the stress on the switches, since it eliminates the need for an excessive duty cycle.

It was found during the literature survey that the source voltage necessary to reduce torque ripple in a BLDC motor is four times the back EMF. Therefore, a torque ripple reduction control based on a Z-source is implemented to achieve this DC voltage. By adjusting the duty cycle of switches in the qZS with ASL and SC converter, we can produce a controlled direct current link voltage (DCLV) that is four times the back-EMF. The voltage is applied to the voltage source inverter (VSI). To address the deficiencies of the initial design of DC-DC converter, such as the precipitous input current and excessive voltage stress on capacitors, quasi-Z-source networks were proposed, which exhibited an identical boost factor. In this article, the circuit topology uses active switched inductor and switched capacitor-based high gain QSZ DC-DC converter. The voltage gain of the converter is given by $3 - D/1 - 2D$, which will be used to achieve the required voltage during the commutation at only 14% of the duty ratio. The proposed system enhances the drive's performance by minimising torque fluctuations and improving stator currents. The converter used in the suggested system can function over an extensive voltage range while maintaining a consistent maximum duty cycle. It significantly lowers the voltage and current stresses on the power switches. Therefore, power switches with a low voltage rating can be used to reduce power loss. Additionally, there is minimal current ripple, and the input current stays continuous.

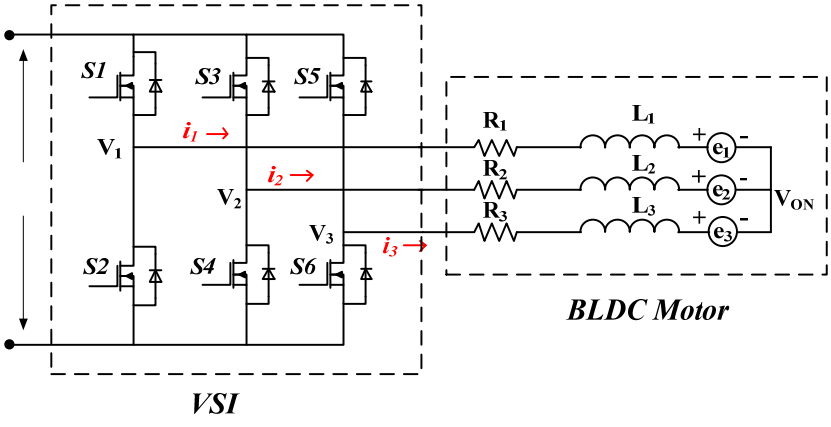
The paper is organised in the following structure: Section 2 discusses the mathematical modelling, electromagnetic torque, rise time, fall time, commutation interval, and torque disturbance of the BLDC motor. Section 3 addresses the proposed topology and suggested DC-DC converter, i.e., active switched inductor (ASI) and switched capacitor (SC)-based QZS DC-DC converter. Additionally, the control strategy to reduce ripple is discussed in this section. Section 4 compares the simulation results of

the proposed topology and those of a traditional BLDC motor. The conclusion is presented in Section 5.

2 Mathematical model of BLDC motor

Generally, in BLDCM, the three-phase star connected-type stator is chosen (Xia et al., 2020; Mohanraj et al., 2022a). A 3-phase VSI-driven BLDC motor's equivalent circuit is depicted in Figure 1. A BLDC drive typically comprises a permanent magnet BLDC motor, an inverter, and a DC supply.

Figure 1 Classical BLDCM drive system (see online version for colours)



For a BLDC motor with a three-phase stator winding, the per-phase voltage equations may be expressed as

$$\left.\begin{aligned} V_1 - V_{ON} &= R_1 i_1 + L_1 \frac{di_1}{dt} + M \frac{d(i_2 + i_3)}{dt} + e_1 \\ V_2 - V_{ON} &= R_2 i_2 + L_2 \frac{di_2}{dt} + M \frac{d(i_1 + i_3)}{dt} + e_2 \\ V_3 - V_{ON} &= R_3 i_3 + L_3 \frac{di_3}{dt} + M \frac{d(i_1 + i_2)}{dt} + e_3 \end{aligned}\right\} \tag{1}$$

For balance 3 phase star connection

$$i_1 + i_2 + i_3 = 0$$

The neutral voltage is represented by V_{0N}. The phase voltages are V_1, V_2, and V_3. Phase currents in the stator are denoted by i_1, i_2, and i_3. L_1, L_2, and L_3 are the motor's self-inductance; e_1, e_2, and e_3 are the trapezoidal-shaped back-EMF; and R_1, R_2, and R_3 are the per phase resistances and M is the mutual inductance of BLDCM. The torque (electromagnetic) of the BLDC motor may be given by:

$$\tau_{ele}^{at_{com}} = \left\{\frac{2E_m}{\omega_m} I_m\right\} + \left\{\frac{2E_m}{\omega_m} * \frac{V_s - 4E_m}{3L_{eq}} * t_{com}\right\} \tag{2}$$

The initial component in the equation reflects a constant torque, whereas the subsequent component represents torque fluctuations. The calculation of the resultant torque ripple is as follows:

$$\tau_{ele}^{ripple} = \tau_{ele}^{at_{com}} - \tau_{ele}^{pre_{com}} = \frac{V_s - 4E_m}{3L_{eq}} * t_{com} \tag{3}$$

According to the given equation (3), a zero second term is required to reduce the torque ripple. Once we have equalled the term to zero, we have $V_{inv} = 4E_m$. We can conclude that to reduce the amount of torque ripple, the rise time T_{rise} of the incoming phase current should be equal to the fall time T_{fall} of the departing phase current. The rotor speed of the motor is directly proportional to the back electromagnetic field (EMF), which fluctuates based on the state of operation of the motor. During the non-commutation period, when the rate of current is zero, the torque is equal to $2EI/\omega m$. Nevertheless, it is essential to adjust the voltage of the DC link throughout the commutation period to maintain a balance between the current decrease and increase rate. To reduce the amount of torque fluctuations that occur BLDCM, this article presents a unique circuit architecture that incorporates an active switched inductor and switched capacitor QZS-based DC-DC converter, in addition to a three-phase inverter and DCLV (DC link voltage) switch.

3 Proposed circuit topology

As shown in Figure 2, power MOSFETs are used in the construction of the qZS DC-DC converter circuits with active switched inductors, switched capacitors, and DCLV selector circuits. By adjusting the duty cycle of switches S_1 and S_2 in the qZS with ASL and SC converter, we can produce a controlled direct current link voltage (DCLV) four times the back-EMF ($V_{inv} = 4E_m$). The voltage applied to the voltage source inverter (VSI), denoted as V_{inv}, can be modified by manipulating the switches S_{in} and S'_{in}. During the commutation process, the S_{in} switch is deliberately turned on to choose the output voltage (V_{inv}) of the qZS with ASL and SC converter as the input voltage ($V_{inv} = 4E_m$) for the VSI. The S_{in} switch is activated both before and after the commutation intervals, delivering power from the supply voltage to the VSI.

3.1 Active switched inductor and switched capacitor-based QZS DC-DC converter

A new DC-DC converter design based on a quasi-Z source converter incorporates A-SL and SC structures. The converter is specifically designed for high-gain conversion. This converter enhances the voltage gain without changing the qZS network. Furthermore, the source current stays continuous with less current ripple. It also decreases the stress on the power switches. Consequently, low rating power switches might be chosen to reduce power loss. The common ground is established using a SC structure, even when A-SL is used. The load will be directly powered by the input source and the capacitor in the qZS network by utilising the SC structure. This results in a decrease in the stress on the devices and an enhancement in efficiency. Furthermore, it prevents any possible resonance between the switches' parasitic capacitor and the inductors (Li and Chen, 2023).

Figure 2 Block diagram of the proposed control strategy of the BLDCM drive

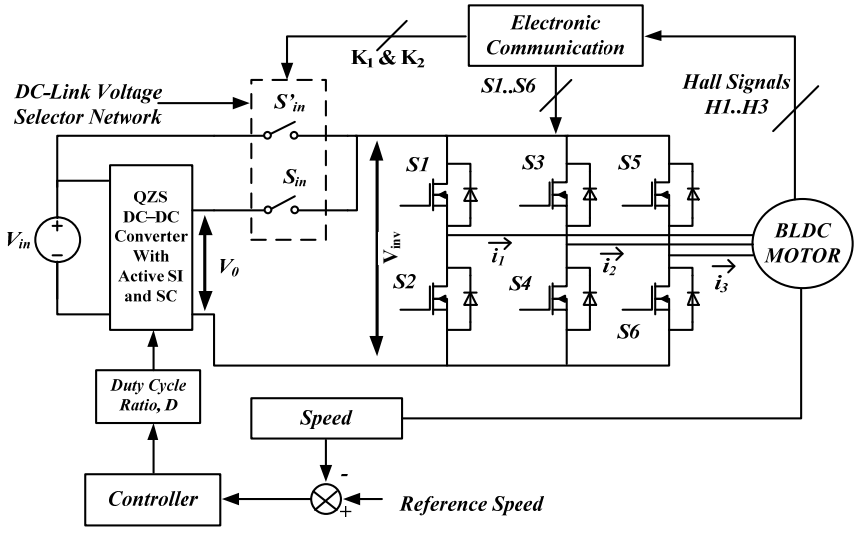
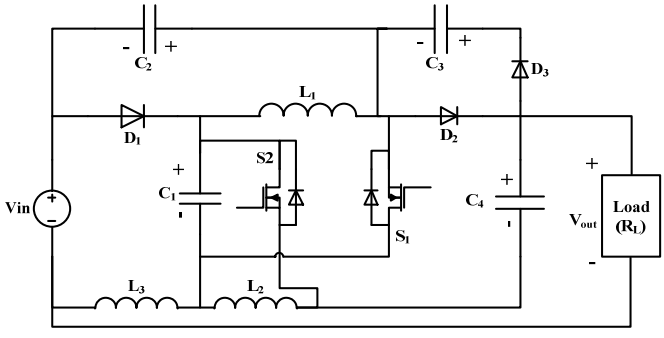


Figure 3 shows QZS DC-DC converter with ASI and SC. At the same time, the same control signal is used to control both switches (S_1 and S_2) simultaneously. It is assumed that all devices are ideal for the converter's analysis. This means that we neglect the forward voltage drops, switches' ON-state resistance, and any components' parasitic characteristics. Capacitors are expected to maintain a constant capacitance and voltage during a single switching period. Each inductor has the same inductance and is large enough to ensure that the converter operates in continuous conduction mode (CCM). The converter operates in two states depending on the switching states of the two power switches that work together.

Figure 3 QZS-based DC-DC converter with ASI and SC



The operation of both states is shown in Figures 4 and 5. During the on state, both switches S_1 and S_2 are in the on position, while diodes (D_1 and D_2) are in the off state and diode (D_3) is in the on state. Inductors (L_1 and L_2) get charged from the capacitor (C_1) through switches (S_1 and S_2), respectively. L_3 is energised by the direct current (DC) source, while S_1 charges C_2. On the other hand, C_3 is charged by C_1 and C_4 through S_1 and S_2.

Figure 4 Equivalent circuit of suggested converter during ON state

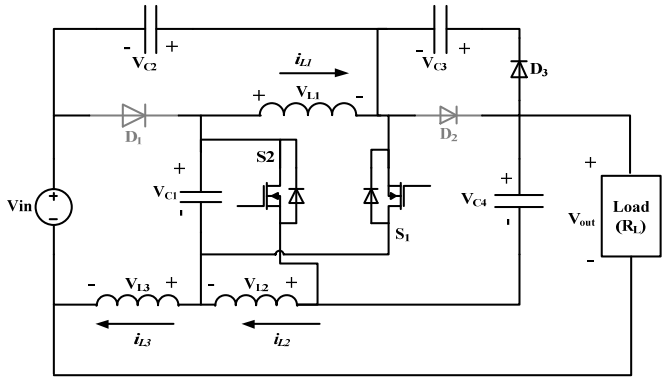
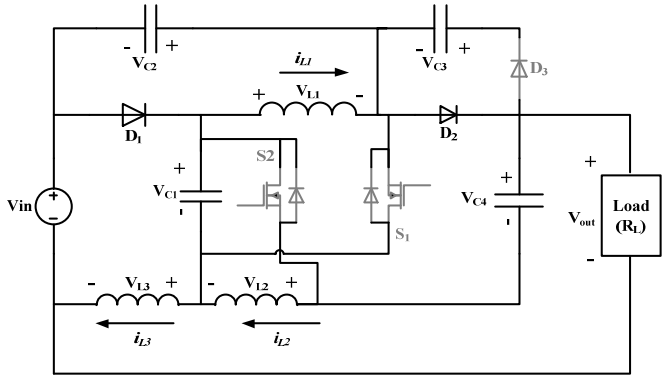


Figure 5 Equivalent circuit of suggested converter during OFF state



Simultaneously, C_1, C_2, and the direct current source collectively supply power to the load R through switches S_1 and S_2. Therefore, by utilising KVL, the voltages across inductors may be determined as follows:

$$V_{L1} = V_{L2} = V_{C1} = V_{C3} - V_{C4} \tag{4}$$

$$V_{L3} = V_{out} - V_{C3} = V_{in} + V_{C2} \tag{5}$$

$$\begin{cases} C_1 \dfrac{d_{Vc1}}{d_t} + C_3 \dfrac{d_{Vc3}}{d_t} + I_0 + i_{L1} + i_{L2} = 0 \\ C_2 \dfrac{d_{Vc2}}{d_t} + I_{in} = 0 \\ C_3 \dfrac{d_{Vc3}}{d_t} + C_4 \dfrac{d_{Vc4}}{d_t} + I_0 = 0 \\ C_4 \dfrac{d_{Vc4}}{d_t} - C_1 \dfrac{d_{Vc1}}{d_t} - i_{L1} - i_{L2} = 0 \end{cases} \tag{6}$$

During OFF state S_1 and S_2 are in the OFF position, while diodes D_1 and D_2 are in the active state and diode D_3 is in the off state. C_1 is charged L_3, and the direct current source by D_1. C_2 is charged by L_1 through D_1. The DC source, together with L_1, L_2, and L_3 connected in series, charges capacitor (C_4) through diodes (D_1 and D_2). Simultaneously, the DC source and inductor (L_1) supply energy to capacitor (C_3) and load RL connected in series by diode (D_1). Therefore, by utilising KVL and KCL, the values of the voltages across inductors and currents across capacitors are determined.

$$V_{L1} = V_{L2} \tag{7}$$

$$V_{L2} = V_{C1} - V_{C2} - V_{C4} \tag{8}$$

$$V_{L3} = V_{in} - V_{C1} \tag{9}$$

$$\begin{cases} C_1 \dfrac{d_{Vc1}}{d_t} + i_{L2} - i_{L3} = 0 \\ C_2 \dfrac{d_{Vc2}}{d_t} + I_0 - i_{L1} + i_{L2} = 0 \\ C_3 \dfrac{d_{Vc3}}{d_t} + I_0 = 0 \\ C_4 \dfrac{d_{Vc4}}{d_t} - i_{L2} = 0 \end{cases} \tag{10}$$

When we apply the voltage-second balancing principle to L_1 and L_2, we get the following equation:

$$DV_{C1} - (1-D)V_{C2} = 0$$

$$D(V_{C3} - V_{C4}) + (1-D)(V_{C1} + V_{C2} - V_{C4}) = 0$$

$$D(V_{out} + V_{C3}) + (1-D)(V_{in} - V_{C1}) = 0$$

$$\begin{cases} V_{C1} = \dfrac{1-D}{1-2D} V_{in}, \quad V_{C2} = \dfrac{D}{1-2D} V_{in} \\ V_{C3} = \dfrac{2}{1-2D} V_{in}, \quad V_{C4} = \dfrac{1+D}{1-2D} V_{in} \end{cases} \tag{11}$$

$$V_{out} = \frac{3-D}{1-2D} V_{in} \tag{12}$$

For the power switches and diodes, the voltage stresses can be calculated as follows:

$$V_{st1} = V_{st2} = \frac{1}{1-2D} V_{in} \tag{13}$$

$$\left.\begin{aligned} V_{D1} &= \frac{1}{1-2D} V_{in} \\ V_{D2} &= V_{D3} = \frac{2}{1-2D} V_{in} \end{aligned}\right\} \tag{14}$$

When comparing the recommended converter to the conventional qZS-based boost converter, the maximum duty cycle remains unchanged. On the other hand, certain qZS network-based converters have excessive duty cycles since they are thought to be narrow, which forces them to operate at high voltage gains. The output voltage will thus be significantly impacted by even a little variation in the duty cycle. Noise would also be a drawback of the narrow switching pulse. To illustrate the superior performance of the proposed converter, it is imperative to conduct a thorough comparison with other high step-up DC-DC converters. The static voltage gain, input resistance, duty cycle required to achieve $4E_m$ (%), inductance and capacitance of each topology are all listed in Table 1. The expressions for inductance and capacitance are made easier by naming two factors, ki and kv.

Figure 6 Comparison of the proposed converter's voltage gain and other high gain converters (see online version for colours)

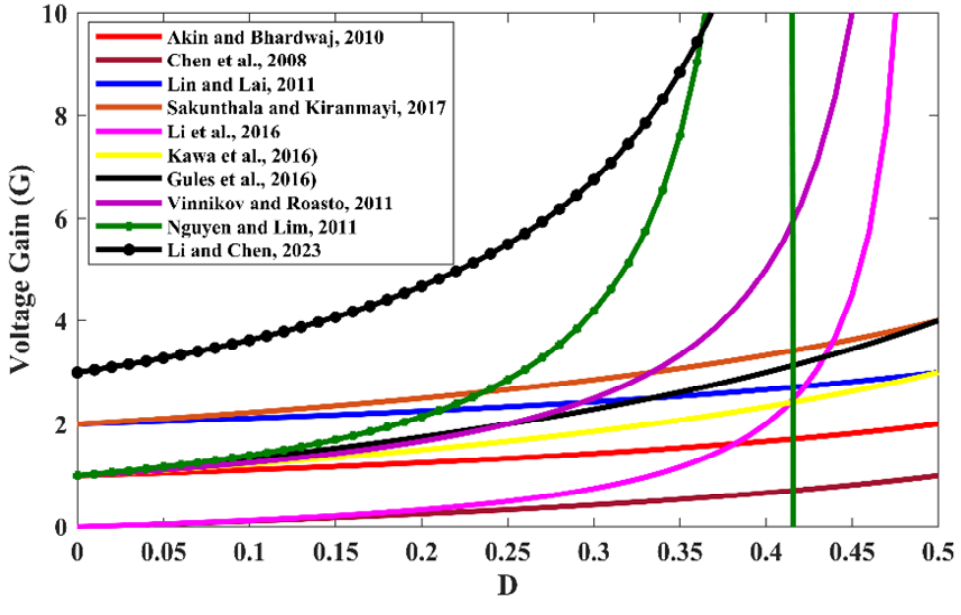


Table 1 Comparison between the converter that is being proposed and other high gain converters

Converter topology	*Static gain (G)*	$R_i = \frac{V_{in}}{I_{in}}$	*Duty cycle required to achieve $4E_m$ (%)*	*Inductance (L)*	*Capacitance (C)*
Boost converter (Akin et al., 2013)	$\frac{1}{1-D}$	$(1-D)^2 R_L$	75	$K_i * D$	$K_C * D$
Buck-boost converter (Chen et al., 2008)	$\frac{D}{1-D}$	$\frac{(1-D)^2 R_L}{D^2}$	80	$K_i * (1-D)$	$K_C * D$
Classical Luo converter (Lin and Lai, 2011)	$\frac{2-D}{1-D}$	$\frac{(1-D)^2 R_L}{(2-D)^2}$	67	$K_i * D$	$K_C * D$
SL-Luo converter (Sakunthala and Kiranmayi, 2017)	$\frac{2}{1-D}$	$\frac{(1-D)^2 R_L}{2^2}$	50	$K_i * D$	$K_C * D$
Classical SEPIC converter (Li et al., 2016)	$\frac{D}{1-D}$	$\frac{(1-D)^2 R_L}{D^2}$	80	$L_1 = L_2 = \frac{K_i * D}{2}$	$C_1 = C_2 = K_c * D$
M-SEPIC converter (Kawa et al., 2016)	$\frac{1+D}{1-D}$	$\frac{(1-D)^2 R_L}{(1+D)^2}$	60	$L_1 = L_2 = \frac{K_i * D}{2}$	$C_1 = C_2 = K_c * D$
M-SEPIC converter (Gules et al., 2016)	$\frac{1+2D}{1-D}$	$\frac{(1-D)^2 R_L}{(1+2D)^2}$	50	$L_1 = L_2 = L_3 = \frac{K_i * D}{2}$	$C_1 = C_2 = K_c * D$
Quasi Z source converter (Vinnikov and Roasto, 2011)	$\frac{1}{1-2D}$	$(1-2D)^2 R_L$	37.5	$L_1 = L_2 = \frac{K_i * D(1-2D)}{(1-D)}$	$C_1 = C_2 = K_c * \frac{(1-D)^2}{(1-2D)}$
Switched inductor quasi Z source converter (Nguyen et al., 2011)	$\frac{1+D}{1-2D-D^2}$	$\frac{(1-2D-D^2)^2}{(1+D)^2} R_L$	28	$L_1 = \frac{K_i * D(3D^2+2D-3)}{4*(1-2D-D^2)}$ $L_2 = L_3 = \frac{K_i * D(D^2+4D-3)}{4*(1-2D-D^2)}$	$C_1 = \frac{K_c * D(1-2D-D^2)}{(1+D)^2}$ $C_2 = \frac{K_c * D(1-2D-D^2)}{(1+2D-D^2)}$
QZS DC-DC converter with ASI and SC (Li and Chen, 2023)	$\frac{3-D}{1-2D}$	$\frac{(1-2D)^2}{(3-D)^2} R_L$	14	$L_1 = L_2 = \frac{K_i * 4D(1-D)}{3*(1-2D)}$ $L_2 = \frac{K_i * 4D(1-D)}{(1-2D)}$ $L_3 = \frac{K_i * D(1-D)(3-D)}{(2+D)(1-2D)}$	$C_1 = \frac{K_c * 5(1-2D)(1+D)}{4(3-D)}$ $C_2 = K_c * (1-2D)$ $C_3 = \frac{K_c * (1-2D)^2 (1-D)}{2(3-D)}$ $C_4 = \frac{K_c * (1-2D)(1-D)}{4(1+D)}$

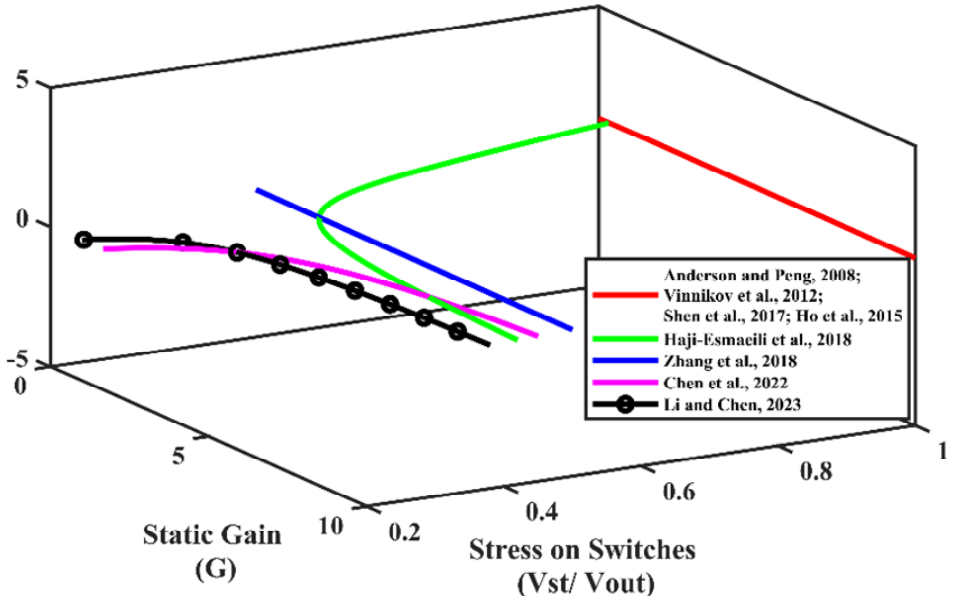
The voltage gain, component count, voltage stress across power switches, and input current behaviour are all listed in Table 2. The components in the suggested converter experience relatively low voltage stress when the same output voltage is required; however, the converter can provide higher voltage gain than other converters under the same duty ratio operating condition, and the duty cycle is not limited as it is with the traditional qZS-based converter.

Table 2 Comparative performance analysis of various high gain Z source DC-DC converters

High gain DC-DC converter	*List of components*					*Input current*	*Static gain*	*Voltage stress on switches*
	C	*L*	*D*	*S*	*Total*			
Quasi-Z-source (Anderson and Peng, 2008)	3	2	2	1	8	Continuous	$G = \frac{1}{1-2D}$	$V_{st} = V_{out}$
Cascaded quasi-Z source (Vinnikov et al., 2012)	5	3	3	1	12	Continuous	$G = \frac{1}{1-3D}$	$V_{st} = V_{out}$
Hybrid Z-source boost (Shen et al., 2017)	5	3	3	1	12	Discontinuous	$G = \frac{1}{1-3D}$	$V_{st} = V_{out}$
Extended boost active-switched capacitor/ switched-inductor quasi-Z source (Ho et al., 2015)	2	2	6	2	12	Discontinuous	$G = \frac{1+D}{1-3D}$	$V_{st} = V_{out}$
High step-up quasi-Z source (Haji-Esmaeili et al., 2018)	7	3	5	1	16	Discontinuous	$G = \frac{2+D}{1-2D}$	$V_{st} = \frac{2G+1}{5G} V_{out}$
Quasi-Z source boost DC-DC converter with high voltage-gain (Zhang et al., 2018)	5	2	4	1	12	Continuous	$G = \frac{2}{1-2D}$	$V_{st} = \frac{V_{out}}{2}$
Common ground quasi-Z-source series DC-DC converters (Chen et al., 2022)	5	2	4	1	12	Continuous	$G = \frac{3-2D}{1-2D}$	$V_{st} = \frac{G-1}{2G} V_{out}$
Proposed converter (Li and Chen, 2023)	4	3	3	2	12	Continuous	$G = \frac{3-D}{1-2D}$	$V_{st} = \frac{2G-1}{5G} V_{out}$

The voltage stress on the power switch vs. voltage gains G for the suggested and similar qZS-based high step-up converters is compared in Figure 6. The graph illustrates how the power switches in the suggested converter would withstand less voltage stress when the same voltage gain G was needed.

Figure 7 Comparison of voltage stress on switches used in high gain S-Source DC-DC converters (see online version for colours)



3.2 Control strategy to reduced commutation ripple

Maintaining an exact DC-link voltage of 4Em during commutation is important to minimise torque ripples in BLDC motors. The topology used for achieving $4E_m$ voltage during commutation is shown in Figure 2. The output voltage of the DC-DC converter is regulated by adjusting the duty cycle of the switch (S_{in}). Sin links the converter's output to the DC supply during the commutation. The BLDC motor's back EMF E_m is directly proportional to speed. The duty cycle ratio D for switches S_1 and S_2 is adjusted to minimise the torque ripple during commutation. The duty cycle equation may be computed as

$$V_{inv} = 4E_m \tag{15}$$

$$D = \frac{3V_{inv} - 4K_{be} * \omega_m}{V_{inv} - 8K_{be} * \omega_m} \tag{16}$$

In each cycle, the brushless DC motor experiences six commutation occurrences. The switch S_{in} is on at the beginning of each commutation period and deactivated by computing T_{fall}. The switch S_1 and S_2 receives the duty ratio D, which is determined by utilising equation (16). V_{in}'s direct current (DC) supply is directly linked to the 3-phase inverter bridge via a switch S'_{in}.

The signal generated by the Hall effect sensors serves as an initial basis for determining the start of the commutation period. The controller, connected to the hall signal, detects the rising and falling ends of the signals. The controller estimates the rotor speed and timing of commutation by analysing the hall signals' rising and falling ends using combinational logic. The switch S_{in} is switched on and the counter starts counting

from zero at the start of each commuting time and during this time S'_{in} is in off condition. The rise and fall periods of both the in and out phase currents determine the maximum value of the counter. The controller computes the duration of time needed for both the increase and decrease of a signal to establish the highest possible value of the counter. This value then decides how long the switch S_{in} will be conducting after that switch S_{in} is disconnected and the counter value is reset after the completion of the commutation cycle. The switch S_{in} is not triggered until the speed reaches the next steady-state value and transitions between two constant speeds. To provide a smooth transition of speed, switch S_1's duty ratio is adjusted during speed variation to keep the DC-link voltage at its maximum value.

4 Simulation result

MATLAB/Simulink was used to simulate the proposed BLDC drive. Table 3 displays the circuit topology's desired parameters. A MATLAB/Simulink model was used to verify the design of the QZS DC-DC converter with ASI and SC. As the induced EMF is a function of speed, at a rotational speed of 1,200 RPM, the duration of the phase's conduction period is roughly 2.7 ms. The duration of the commutation interval reduces as the speed increases. The converter maintains a steady voltage at the DC connection during the transient period to provide high-speed operation. Nevertheless, the quasi-Z-source converter, equipped with an active switching inductor and active capacitor, has a more rapid reaction when compared to other converters employed in similar systems, as demonstrated in Cao et al. (2019) and Shi et al. (2010).

Table 3 Parameters of the BLDCM drive system

Parameter	*Values*
Power rating	325 W
Input voltage	24 V
Torque constant	0.11 N-M/A_Peak
Resistance of motor	0.5 ohm
Inductance of motor	0.89 mH
Rated current	4.5 A
Switching frequency of SL-qZS converter	50 kHz
Source voltage	24 V
Output voltage	100 V
Duty ratio	0.15
Capacitance ($C_{1,2,3,4}$)	50 µF
Inductance ($L_{1,3}$)	500 µH
Inductance (L_2)	3 mH
Switching frequency	50 kHz

The efficiency of the converter for 50 KHz at given parameters has been calculated as 92.67% at 24-V input voltage and 325 watt. The simulation results for the BLDCM without DC-DC converter operating at its rated voltage and 1.5 N-m rated torque are

shown in Figures 8 and 9. The simulation results of the BLDCM clearly indicate that the torque ripple is large in the absence of any converter. The ripple in torque is around 50% of the load torque.

Figure 8 Phase current I_a of BLDC motor at 1,200 RPM without a DC-DC converter

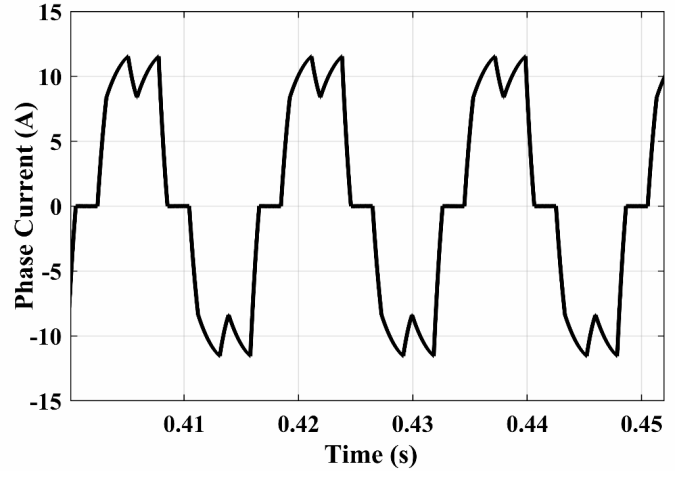
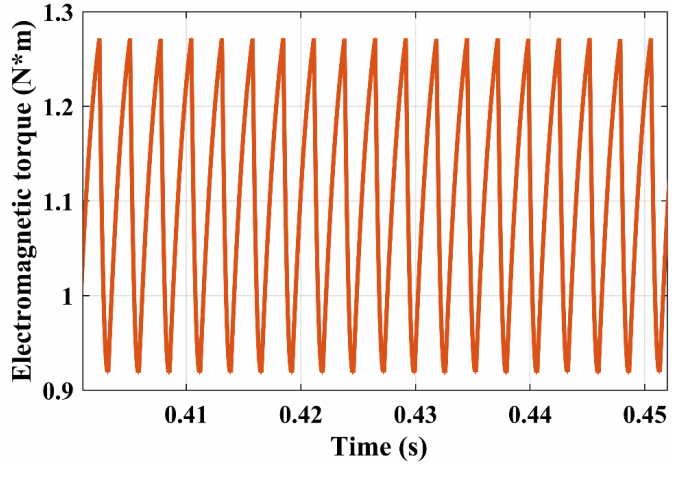


Figure 9 Electromagnetic torque of BLDC motor without a DC-DC converter (see online version for colours)



Figures 10 and 11 depict the simulation results of the BLDCM with simple boost converter used to suppress torque ripples. For the same rated torque, the torque tipple is around 25% for direct current (DC) supply voltage of 24 V.

Figure 10 Phase current I_a of BLDC motor with a simple boost DC-DC converter

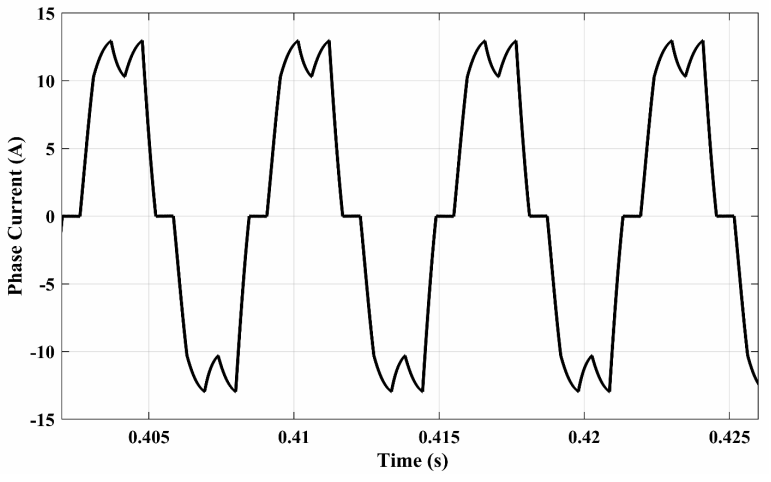
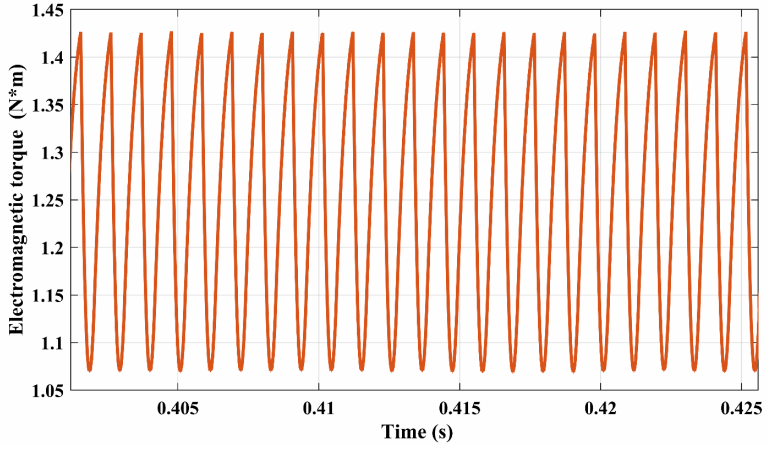


Figure 11 Electromagnetic torque of BLDC motor with a simple boost DC-DC converter (see online version for colours)



Figures 12 to 15 depict the simulation results of phase current, electromagnetic torque, speed, and DC link voltage waveform for the suggested circuit topology. Simulation is performed on a 24 V DC supply voltage and the motor has a load torque of 1.5 N-m. The recommended DC-DC converter's duty ratio is adjusted to raise the required voltage of the applied DC supply voltage. It can be observed that there are fewer fluctuations and that the phase current waveform seems more consistent.

Figure 12 Phase currents of BLDC motor for the suggested DC-DC converter (see online version for colours)

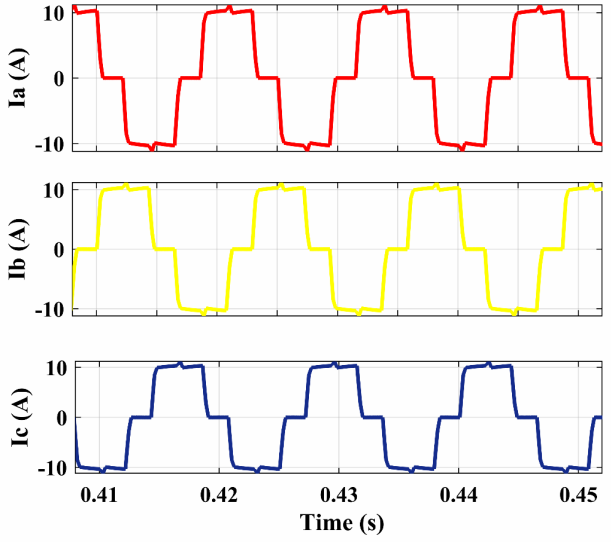


Figure 13 Electromagnetic torque of BLDC motor for the suggested DC-DC converter (see online version for colours)

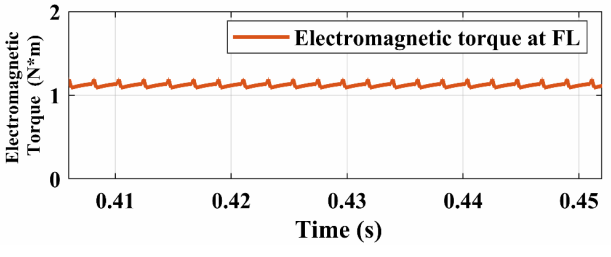


Figure 14 Speed of BLDC motor for the suggested DC-DC converter (see online version for colours)

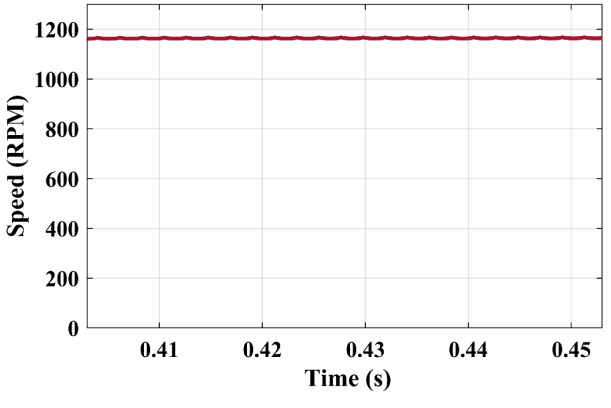
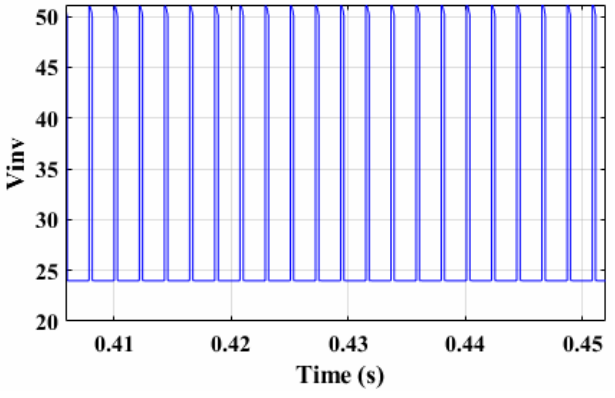
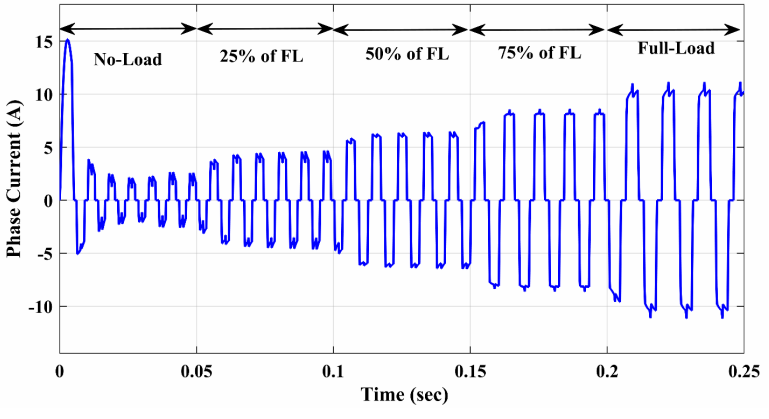


Figure 15 DC-link voltage of BLDC motor for the suggested DC-DC converter (see online version for colours)



A comparison of per-phase current, speed, and torque is also performed for different loading conditions, as shown in Figures 16 and 17. The torque ripple for the suggested converter at full load is about 7%, and at half of the full load is about 12%. However, 75% of the full load's torque ripple is reduced to 6%. Similarly, the current ripple is highest for half of the full load torque and minimum for 75% of the full load. From Figure 17, it is clear that speed is inversely proportional to load, which indicates that the motor is stable during the operation.

Figure 16 Phase current of BLDC motor for the suggested DC-DC converter at different loading conditions (see online version for colours)



The graph of torque ripple size of the suggested converter for different loading conditions are shown in Figure 18. The torque ripple is reduced by increasing the load on the drive. The peak gives the torque ripple-to-peak ratio and average torque value. From the results, it is calculated that at full load condition, its value is only 7.43% and at the no-load condition is equal to 95.53%. There is a significant change in torque ripple if we move from 75% of FL to 50% of FL.

Figure 17 Speed (RPM) and electromagnetic torque (N-m0 of BLDC motor for the suggested DC-DC converter at different loading conditions (see online version for colours)

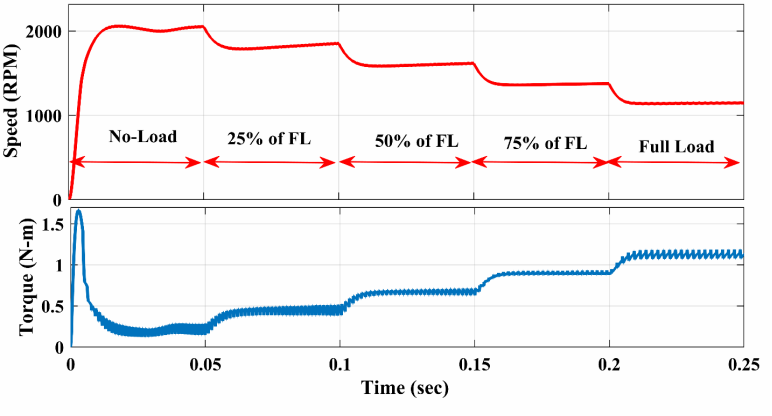


Figure 18 Torque ripple size of suggested converter for different loading conditions (see online version for colours)

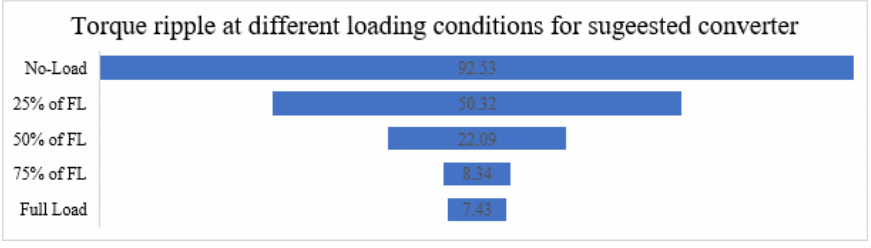
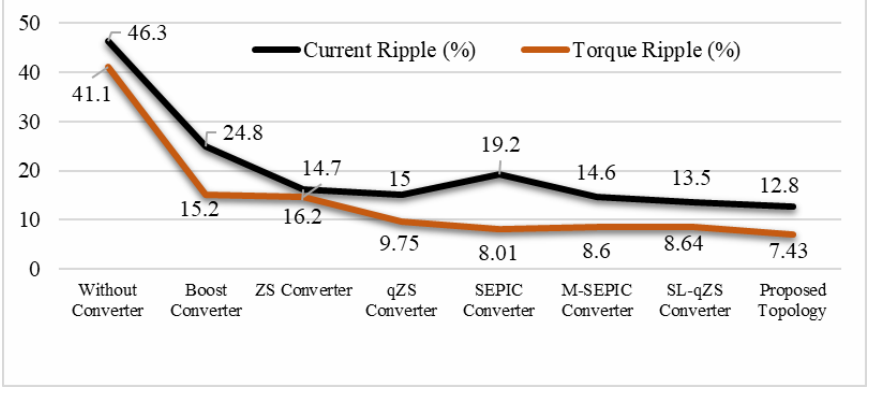


Figure 19 Comparison of current and torque ripples of different BLDC topology (see online version for colours)



The suggested topology possesses several interesting characteristics, notably a design that efficiently reduces current ripple. Compared to previous control strategies, the proposed approach shows a significant decrease in the current ripple, at over 34%. The circuit's switching loss is decreased since the converter's desired output is only attained at a 14%

pulse width. Improved computational efficiency is achieved by the proposed control strategy, which lowers commutation current fluctuation without utilising any PWM systems. The converter requires smaller magnetic components, which lowers the driving system's weight. The converter switch will experience less stress because of the higher boosting ratio's decreased requirement for high-duty cycle operation. The complete comparative study was carried out between the proposed technique and other established approaches for reducing torque ripple in BLDC drive. From the above figure it has been observed that the prosed method exhibits minimum torque ripple and current ripple (7.04% and 12.8%) compared to SLQZS (8.64% and 13.5%), M-SEPIC (8.6% and 14.6%), SEPIC (8.01% and 19.2%), QZS (9.75 and 15 %), ZS (14.7% and 16.2%), boost converter (15.2% and 24.8%) and without DC-DC converter (41.1% and 46.3%) techniques. A comparative chart proposed topology of BLDC drive for full load operation with different DC-DC converters is shown in Figure 19.

5 Conclusions

Active switched inductor and switched capacitor-based QZS DC-DC converter architecture is beneficial for drive systems in which the motor's rated voltage exceeds the available DC supply voltage. The suggested module decreases the current and torque ripple by around 34%. Torque ripple for the suggested converter at about 7.43% and at half of full load about 22%. This demonstrates the effectiveness of the suggested control method. The proposed converter's integrated A-SL and SC structure greatly increases the voltage gain without changing anything inside the qZS network, allowing it to operate over a wide voltage range and maintain a constant input current with less current and torque ripple. Moreover, smaller magnetic element sizes were needed, which decreased the drive system's weight. By reducing the necessity for excessive duty cycle operation, the high-gain converter will reduce the stress put on the converter switch. It also reduces the current and voltage stress on the power switches. The converter's efficiency is 92.63%, and the minimum voltage stress is among similar kinds of quasi-Z source converters.

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