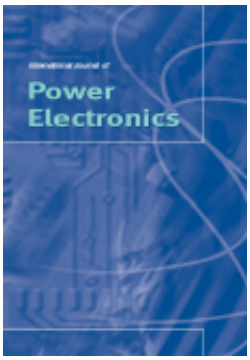


International Journal of Power Electronics

ISSN online: 1756-6398 - ISSN print: 1756-638X
https://www.inderscience.com/ijpelec

On the common mode current reduction in induction motor fed by three-level NPC inverter for pumping photovoltaic application

Zouhaira Ben Mahmoud, Adel Khedher

DOI: 10.1504/IJPELEC.2025.10067953

Article History:

Received:	25 March 2024
Last revised:	07 July 2024
Accepted:	14 July 2024
Published online:	15 January 2025

On the common mode current reduction in induction motor fed by three-level NPC inverter for pumping photovoltaic application

Zouhaira Ben Mahmoud* and Adel Khedher

LATIS – Laboratory of Advanced Technology and Intelligent Systems,
Ecole Nationale d'Ingénieurs de Sousse,
Université de Sousse,
4023, Sousse, Tunisia
Email: benmahmoud_zouhaira@yahoo.fr
Email: adel_kheder@yahoo.fr
*Corresponding author

Abstract: The presence of common mode voltage (CMV) poses a significant challenge in motor drive applications. Particularly, for Photovoltaic Pumping (PVP) systems, the high-frequency fluctuations of CMV can induce a common mode current (CMC). These challenges not only diminish the lifespan and the reliability of the motor and PV panel but also present safety problems. This work suggests a novel space vector modulation (SVM) for three level NPC (3L-NPC) converter fed induction machine (IM). The proposed SVM simplifies the 3L space vector diagram (SVD) to six two level (2L) diagrams. The synthesis of the zero voltage vector is then achieved through a virtual approach, combining two active vectors. The principal features of the latter are low complexity, low computation burden, reduced CMV and leakage current with high DC bus utilisation ratio. The feasibility and effectiveness of the suggested SVM scheme is verified through both numerical tests and FPGA-based real time implementation.

Keywords: PV pumping system; 3L-NPC inverter; SVM; CMV; leakage current; FPGA board.

Reference to this paper should be made as follows: Ben Mahmoud, Z. and Khedher, A. (2025) 'On the common mode current reduction in induction motor fed by three-level NPC inverter for pumping photovoltaic application', *Int. J. Power Electronics*, Vol. 21, No. 1, pp.28–45.

Biographical notes: Zouhaira Ben Mahmoud has received her BE in Electrical Engineering from the National Engineering School of Sfax (ENIS), Tunisia, in 2012. She obtained her PhD in 2019. Currently, she is a Research Doctor at the Laboratory of Advanced Technology and Intelligent Systems (LATIS), ENISo. Her fields of interest are power converters, renewable energy, grid integration, power transmission and induction machine.

Adel Khedher is a Professor in Electrical Systems in the Industrial Electronic Engineering Department of ENISO. He received his PhD and HDR from ENIS in 2006 and 2012. From September 2010, he has been an Associate Professor in the Industrial Electronic Engineering Department of ENISO, Sousse, Tunisia. He has been promoted to the Full Professor Grade in Electrical Systems in the same department since November 2012. His research interests include the static converters control, electric machine drives, renewable energy systems and smart grid.

1 Introduction

Photovoltaic (PV) energy has become increasingly popular in a variety of applications, mainly in pumping systems (Zarrad et al., 2019; Sunil Kumar and Rajan, 2023; Sonak and Bhim, 2015). In rural areas, standalone PV pumping (PVP) unit is commonly applied because grid connection may be costly and complicated (Sunil Kumar and Rajan, 2023). The significant advantages of PVP systems include not only the avoidance of traditional energy depletion and its environmental impact but also the reduced maintenance requirements when compared to diesel water pumping systems (Saoudi et al., 2021). Various kinds of motors have found utilisation in the PVP applications. The induction motor (IM) is highly preferred for these PVP systems because of its several benefits notably straightforward structure, maintenance-free nature, and high efficiency (Zarrad et al., 2019; Saoudi et al., 2021).

In general, the PVP system incorporates a power converter that converts convert the DC energy delivered by the PV panel to the AC energy transferred to the IM, which is, in turns, connected with centrifugal pump. Indeed, using this level of inverter is anticipated to tackle issues related to power quality, and there have been reports of it causing an elevation in both losses and the intensity of ripples in the motor current. The main concern associated with harmonics, which directly impacts the flow rate of the PVP system, can be readily resolved by adopting multi-level inverters (MLIs). Indeed, the use of MLIs exhibit lower dv/dt stresses on the output terminal, alleviated electromagnetic interference, lower common mode voltage (CMV) and require low filters, reducing the stress on the motor's bearings and preventing its potential damage (Mahmoud et al., 2017a). Among the different MLIs configurations utilised with motor drives, the three-level neutral point clamped (3L-NPC) inverter has stood out as the most widely adopted inverter topology (Guo et al., 2021).

The connection between the IM neutral point and the DC link midpoint of the NPC converter leads to the creation of the CMV issue, which poses a significant drawback in motor drive applications (Mansuri et al., 2023; Chinthamalla et al., 2016). This phenomenon adversely affects critical aspects such as motor reliability. Nearly half of the failures and degradation in bearings can be attributed to the CMV. Specifically, for PVP systems with no galvanic isolation, high-frequency fluctuations in CMV can be occurred. These variations induce a common mode current (CMC) which has the potential to flow to the ground through the leakage circuit. This current detrimentally impacts the output current waveforms, amplifies losses in the overall system, contributes to electromagnetic emissions, as well as reduces the PV panel lifespan (Mahmoud et al., 2019; Jain et al., 2023; Rao et al., 2022).

Numerous research studies have undertaken various efforts to alleviate the impact of CMV by adopting corrective or preventive processes. Many of these studies involve implementing hardware modifications. However, modifying the inverter structure by adding extra components, will lead to a rise in the overall system cost and size, along with increased complexity. Another alternative for CMV mitigation is the software method which is mostly preferred since no additional components are required and then more reliability of the overall system is obtained. The most adopted software solutions are derived from the space vector modulation (SVM) approaches through the adjustment of the pulse patterns and the appropriate space vector selection. The latter allows not only the CMV reduction, but also superior DC-link voltage balancing, self-neutral point

equilibrium, improved-quality harmonics profile, and minimisation of switching losses (Mittal et al., 2012). The traditional SVM technique of the 3L inverter is referred to as nearest three-vectors SVM (NTV-SVM) (Mahmoud et al., 2017b). This modulation technique divides the 3L space vector diagram (3L SVD) to six sectors, each further decomposed into four regions. To achieve the desired output voltage, the NTV-SVM selects the closest three states. In order to limit the CMV amplitude, the latter is modified by excluding the switching state of the zero vector, which produces the highest CMV amplitude (Hava and Ün, 2011). The SVD of the 3L-NPC inverter comprises various types of space vectors, that generate different CMV levels. Based on the space vector's type, three basic SVM approaches have been proposed. Small vectors, when used for generating the reference voltage vector, tend to cause significant fluctuations in CMV. As a result, these vectors are generally excluded and it has been focused exclusively on the adoption of zero, medium and large vectors (Qin et al., 2020). This technique is named as the LMZV method, designed to reduce the CMV amplitude to $\pm V_{dc}/6$. Another approach aims to completely eliminate CMV through the adoption of one zero vector and two medium vectors, as the latter produces zero CMV. This method is referred to as the 2M1ZV method. However, the three medium vectors (3MV) method utilises three neighbouring medium vectors to synthesise the reference vector (Cavalcanti et al., 2012). Although the aforementioned SVM approaches can effectively reduce the CMV or can completely suppress it, they suffer from several drawbacks mainly, the DC bus utilisation ratio and the output current quality.

In this regard, the presented paper aims to deal with the CMV issue in PVP system by firstly exploring the conventional SVM schemes and then, suggesting an improved and simplified SVM scheme that deals with the CMV concern. Compared with the CMV mitigation strategies based on hardware modification, the recommended SVM approach does not require any additional components, leading to more reliability of the whole PVP system. Also, it provides reduced CMC with high current quality and high DC bus utilisation ratio when compared with the current software approaches. The proposed SVM strategy is recommended for transformer-less PVP conversion systems. The adoption of this technique for the latter has several merits:

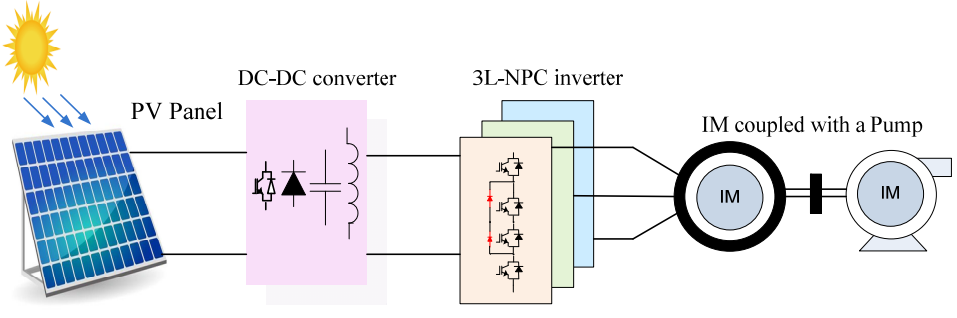
- Compact PVP system: Transformer is often bulky and heavy component. By eliminating the latter, PVP system can be more compact and lightweight.
- Improved reliability: Reducing the CMV increases the motor reliability and the lifespan of PV panels with lower maintenance requirement.
- Compliance with safety standards: PVP system with reduced CMV leads to reduced CMC and hence, avoiding safety problems.

The paper remainder has the following structure. Section 2 presents the PVP system design as well as the CMV problem is raised. In Section 3, the classical SVM schemes are explored. Section 4 is reserved for the suggested SVM with CMV reduction. Simulation and real-time implementation results are conducted in Section 5. Finally, some concluding remarks are drawn in Section 6.

2 PVP system description and CMV issue

In general, the two-stage PVP system is always recommended since it allows the dc bus control with improved dynamic response whatever the solar insolation variations when compared with the single-stage one (Singh and Kumar, 2016). A DC–DC converter is employed in the two-stage configuration in order to implement maximum power point tracking (MPPT) control, with the objective of extracting the maximum power from the PV panel (Boussaada et al., 2023). Meanwhile, the control of the DC-bus voltage is primarily managed by a 2L-VSI. For performance improvement, the 3L-NPC inverter is used instead of the 2L-VSI. The overall structure of the PVP system is depicted in Figure 1. In the first step, the PV panel voltage undergoes conversion to a higher DC-link voltage level through a boost converter which operates at MPP. In the second step, the 3L-NPC inverter converts the high DC voltage to a three-phase AC voltage that is provided to the IM connected to a centrifugal pump. While, the 3L-NPC power converter is controlled by an enhanced SVM scheme that mitigates the CMV issue and optimises the DC-bus voltage utilisation. For a focused analysis, our interest lies only in the AC side, where the 3L NPC inverter is connected to the IM.

Figure 1 Synoptic diagram of a PVP system (see online version for colours)



2.1 IM modelling

The IM electrical model is elucidated in the ($\alpha - \beta$) frame as follows (Saoudi et al., 2021):

$$\begin{cases} \dfrac{d}{dt}X = [A] \quad X + [B]U \\ Y = C \qquad\quad X \end{cases} \tag{1}$$

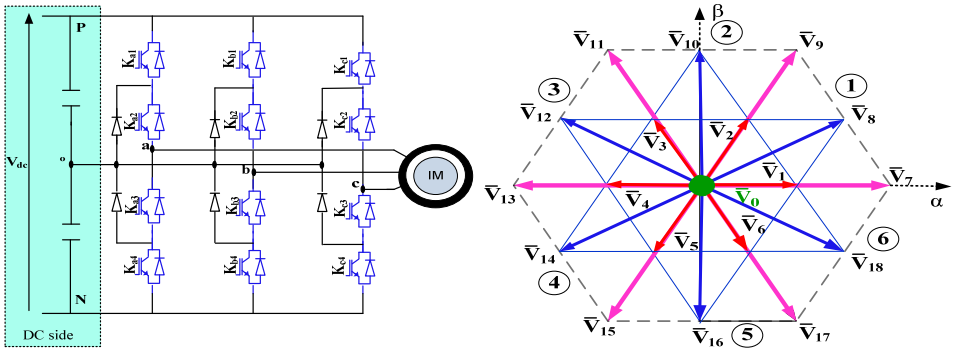
where

$$X = \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \\ \varphi_{s\alpha} \\ \varphi_{s\beta} \end{bmatrix}, U = \begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix}, Y = \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{2}$$

2.2 Three-level NPC inverter topology

The NPC topology introduced by Nabae et al. in 1981 is potentially the earliest commercially implemented multilevel converter worldwide. To establish connections between the midpoint of the upper and the lower legs, clamping diodes are employed, as shown in Figure 2(a). For the 3L configuration, it offers three voltage levels at the output of each phase ($\pm V_{cd}/2$ and 0). The correspondence between output voltage level, switching states and power device status is outlined in Table 1. Considering all combinations of the switching states, 19 space vectors can be provided, constructing the 3L SVD depicted in Figure 2(b). These vectors are categorised into four types: zero, small, medium and large vectors.

Figure 2 (a) 3L NPC electrical circuit (b) 3L SVD (see online version for colours)



(a) (b)

Table 1 Space vectors and produced CMVs

Vector's type	*Vector's group*	V_{CM}
Zero	$\bar{V}_0$	0 (OOO), $\pm V_{dc}/2$ (PPP or NNN)
Small	$\bar{V}_1 - \bar{V}_6$	$\pm V_{dc}/6$; $\pm V_{dc}/3$
Medium	$\bar{V}_8, \bar{V}_{10}, \bar{V}_{12}, \bar{V}_{14}, \bar{V}_{16}, \bar{V}_{18}$	0
Large	$\bar{V}_7, \bar{V}_9, \bar{V}_{11}, \bar{V}_{13}, \bar{V}_{15}, \bar{V}_{17}$	$\pm V_{dc}/6$

2.3 CMV issue in IM

Despite efforts to enhance power converters with improved efficiency, the growing prevalence of the multilevel inverters in electric machines has reignited concerns about a primary issue in these systems which are the CMV (Huang and Li, 2020; Jiang et al., 2020). The elevated switching frequencies of power devices result in increased CMCs that may circulate through leakage circuit paths between the PV panel and the IM frame. The CMV can be mathematically described as (Guo et al., 2021):

$$CMV = V_{no} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) \tag{3}$$

For the conventional 2L-VSI, the CMV can assume four levels: $\pm V_{dc}$ and $\pm V_{dc}/3$. While in the case of 3L-inverter, the CMV level can vary between different values: 0, $\pm V_{dc}/6$, $\pm V_{dc}/3$, $\pm V_{dc}/2$. As results, with the 3L structure, it can be possible to control the CMV level through an adequate selection of the optimised space vector. More specifically, the magnitude of the CMV is contingent upon the space vector category, as demonstrated in Table 1. With the aim to attenuate the induced CMC and comply with the allowable value as defined by the German standards VDE-0126-1-1, CMV magnitude needs to be mitigated. Indeed, for PV systems, the allowable RMS value of this current is limited to 300 mA (Mahmoud et al., 2019).

3 Classical SVM schemes

3.1 NTV-SVM scheme

The NTV-SVM is the common modulation technique used on the 3L inverter. It entails applying the three nearest vectors to each triangle. Similar to 2L-SVM, the 3L-SVM dissects the 3L-SVD of Figure 2 into six fundamental sectors. Each sector is subdivided into four triangles.

After determining the triangle, the synthesis of the reference vector involves utilising the adjacent vectors of the latter. The first sector division of the NTV-SVM scheme as well as the produced CMV for the first triangle are depicted in Figure 3. The CMV variations during transitions from one state to another are also illustrated for each switching sequence. As it is observed, the CMV levels are varied between the levels 0 and $V_{dc}/2$. The highest value of CMV is produced by the zero vectors with the switching states (NNN) and (PPP). Accordingly, to limit the CMV level to a reduced value, it is recommended to neglect these vectors.

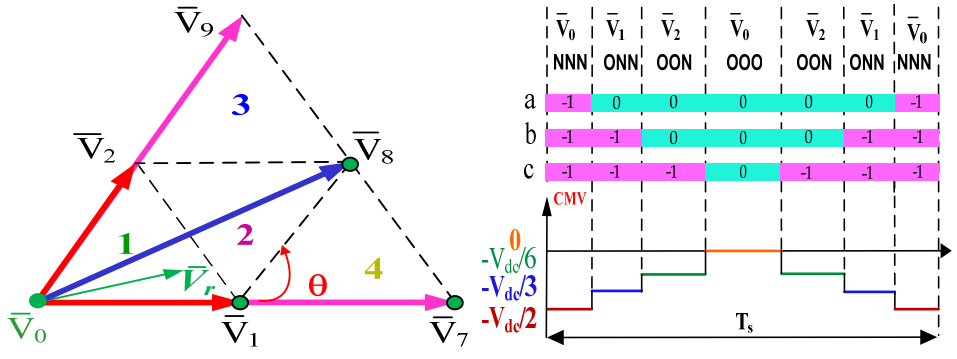
3.2 SVM scheme based on 2L-hexagon

The SVM based on 2L-hexagon is another alternative of 3L-SVM which simplify the 3L-SVD into six 2L-SVD. Therefore, the 3L-SVM can be carried out in a simple manner as the 2L-SVM. The essential step of this scheme is to identify the small hexagon where $\overline{V}_r$ is lying. If the latter is determined, $\overline{V}_r$ is translated to the centre of this small hexagon to obtain a novel reference vector $\overline{V}_n$, as illustrated by Figure 4(a). The latter is inferred from the original vector $\overline{V}_r$, as described in the following equation:

$$\overline{V}_n = \overline{V}_r - \frac{V_{dc}}{3} e^{j(H-1)\pi/3},\ H = 1, \ldots, 6 \tag{4}$$

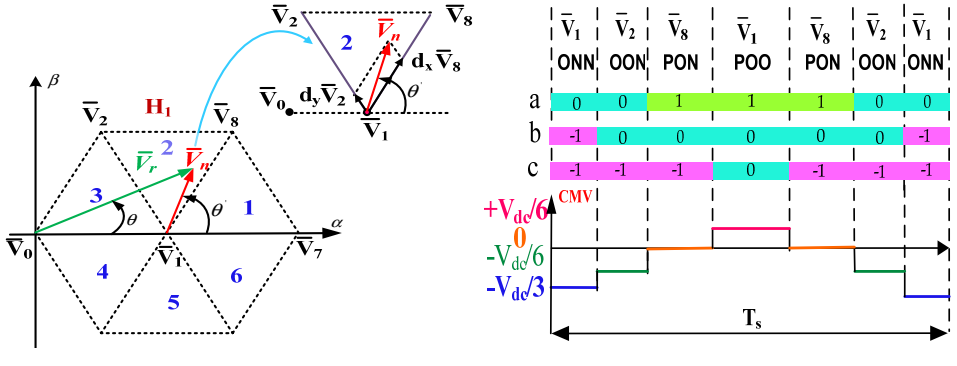
At this stage, it is necessary to pinpoint the subsector that contains the novel constructed vector $\overline{V}_n$, recognise the two suitable neighbouring vectors of the small hexagon, and calculate the timings for their application. The corresponding switching sequences as well as the produced CMV level for the second subsector of the first small hexagon are detailed in the Figure 4(b). It can be seen that the CMV is variable and can reach the amplitude of $V_{dc}/3$.

Figure 3 (a) First sector division in the NTV-SVM (b) The produced CMV (see online version for colours)



(a) (b)

Figure 4 (a) $\bar{V}_n$ synthesis in the hexagon-SVM (b) The produced CMV (see online version for colours)



(a) (b)

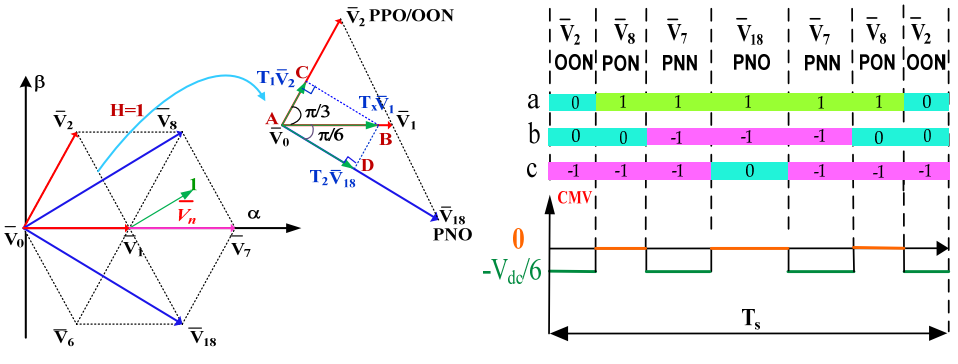
4 Control of IM fed by 3L NPC inverter with CMV reduction

Certainly, when the IM is controlled by the two afore mentioned SVM schemes, important variations in CMV may occur and result in a great leakage current. To prevent the overall conversion system from the adverse consequences of this current, it is imperative to deals with the CMV issue and consider it even during the design stage. For this purpose, in our work, some improvements have been made based on the conventional SVM applied the 2L-hexagon approach. The proposed SVM algorithm can reduce the CMV amplitude without negatively impacting the inverter's performance concerning the utilisation of DC-bus voltage when compared to the available SVM techniques aiming to reduce the CMV. The features of the proposed algorithm can be summarised in its simplicity, less computation burden, low CMV amplitude and thus, low leakage current with high DC bus utilisation ratio. Commonly, it offers better stator current quality.

Based on the illustration presented in Figure 4 and when $\bar{V}_n$ is situated in subsector 1, $\bar{V}_1, \bar{V}_7$ and $\bar{V}_8$ will be selected. The adoption of the following space vectors results in four levels of CMV: the medium vector $\bar{V}_8$ leading to CMV = 0 V; the large $\bar{V}_7$ vector generating a CMV with amplitude equal to $-V_{dc}/6$; and the small vector $\bar{V}_1$ used as zero vector, which provides the levels $+V_{dc}/6$ with the state (POO) and $-V_{dc}/3$ with the state (ONN). To decrease the variations of the CMV levels and their amplitudes, we suggest virtualise the small vector $\bar{V}_1$, which produces the highest CMV amplitude, using two virtually opposite vectors that produce the same CMV. In other words, we create a virtual zero-vector within the two-level hexagon with the same CMV levels as vectors $\bar{V}_8$ or $\bar{V}_7$ (0 or $-V_{dc}/6$). Accordingly, the CMV variations will be minimised and its amplitude will be restricted to $+V_{dc}/6$.

With the aim to obtain an output current with low harmonic content, it is recommended to use the adjacent space vectors for the reference vector synthesis. Taking this into account and according to Figure 5, as can be seen, the adjacent vector to $\bar{V}_7$ is the medium vector $\bar{V}_{18}$ which produces an equal CMV level with the vector $\bar{V}_8$ (0 V).

Figure 5 (a) Novel reference vector synthesis in the proposed SVM (b) The produced CMV (see online version for colours)



(a) (b)

Table 2 Virtualisation of $\bar{V}_1$ when $H = 1$

Subsector's number	$\bar{V}_1$ *is virtualised by*
1	$\bar{V}_2$ (OON) and $\bar{V}_{18}$ (PNO)
2	$\bar{V}_0$ (OOO) and $\bar{V}_7$ (PNN)
3	$\bar{V}_6$ (ONO) and $\bar{V}_8$ (PNO)
4	$\bar{V}_2$ (OON) and $\bar{V}_{18}$ (PNO)
5	$\bar{V}_0$ (OOO) and $\bar{V}_7$ (PNN)
6	$\bar{V}_6$ (ONO) and $\bar{V}_8$ (PNO)

Similarly, the neighbouring vector to $\overline{V_8}$ is the small vector $\overline{V_2}$ that generates the same level of CMV ($-V_{dc}/6$) as the vector when the switching state (OON) is chosen. Consequently, the vectors $\overline{V_{18}}$ and $\overline{V_2}$ which are considered as virtually opposite vectors, will be applied to virtualise the vector $\overline{V_1}$ if $\overline{V_n}$ is situated in the first subsector within the first small hexagon. By extending this concept for all subsectors, the vector is virtualised as detailed in Table 2.

Now, it remains to determine the applied new vectors duration times. Taking the same example of Figure 7 and assuming that T_1 and T_2 are the application times of the vectors $\overline{V_2}$ and $\overline{V_{18}}$, respectively and T_x is the application time of the vector $\overline{V_1}$ within the classical SVM algorithm. According to the geometric representation of Figure 5, we can consider two drawing right-angled triangle ABC and ABD. Given that $\overline{V_1}$ forms an angle of 60° with $\overline{V_2}$ and an angle of 30° with the vector $\overline{V_{18}}$, we can write:

$$\begin{cases} \cos 60° = \dfrac{T_1 V_2}{T_x V_1} \\ \cos 30° = \dfrac{T_2 V_{18}}{T_x V_1} \end{cases} \tag{5}$$

Resolving these equations, we can obtain:

$$\begin{cases} T_x V_1 = 2 T_1 V_2 \\ T_x V_1 = \dfrac{2}{\sqrt{3}} T_2 V_{18} \end{cases} \tag{6}$$

Since $V_2 = V_1$ and $V_{18} = \sqrt{3} V_1$, we can deduce that:

$$\begin{cases} T_1 = \dfrac{T_x}{2} \\ T_2 = \dfrac{T_x}{2} \end{cases} \tag{7}$$

Hence, the selected vectors, used to virtualise the vector $\overline{V_1}$, will be applied with an equal application time. The obtained correlation (7) could be extended to encompass all operational subsectors of $\overline{V_n}$. In the Figure 5(b), the associated switching sequence of the first subsector within the first small hexagon as well as the produced CMV are provided. It is outlined that the highest CMV amplitude is limited to $V_{dc}/6$. On the other hand, the number of level change per switching period is decreased what is crucial for the common current reduction since the latter depends not only on the CMV amplitude but also on its variations.

5 Software and hardware results

5.1 Software results

To assess the performance of the IM under the suggested SVM approach, numerical simulations were conducted using a 3L NPC inverter. The PV generator was substituted with a DC voltage source with V_{dc} = 560 V, to ensure uniform testing under consistent DC-bus voltage conditions. It is important to highlight that changes in the voltage across the DC-bus impact the CMV produced by the inverter. The IM parameters are detailed in Appendix.

Figure 6 IM responses, (a) speed (b) electromagnetic torque (c) stator flux (see online version for colours)

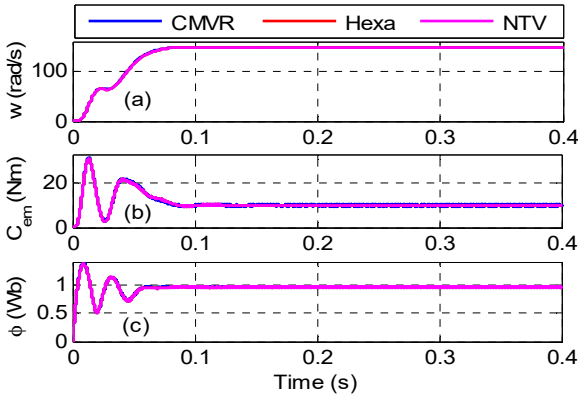


Figure 6 displays the simulated speed, torque and flux responses of the IM controlled with the proposed SVM technique and both conventional ones. For the three SVM approaches, the IM reaches its steady-state operation without oscillations, though they present some ripples with different levels for each approach. To evaluate the quality of the obtained stator current, its total harmonic distortion (THD) is computed and drawn in Figure 7. It is noted that the conventional SVMs present similar result with the lowest THD. The THD acquired with the suggested SVM is the biggest one. In our opinion, the rise in the stator current's THD is caused by the selected space vectors that cannot offer the highest line current quality.

Figure 8 depicts the obtained CMV waveforms using the conventional and the proposed SVM approaches for different values of the modulation index m. For low values of m (m = 0.4 and m = 0.6), the NTV approach produces the highest variations of CMV and the highest amplitude, reaching the value $V_{dc}/2$. While, the hexagon method varies within the range $\pm V_{dc}/3$. The most important results are obtained with the proposed algorithm when the CMV amplitude is limited to $\pm V_{dc}/6$. For high values of m (m = 0.8 and m = 1.15), the NTV and the hexagon method ensure the same results with a CMV amplitude of $\pm V_{dc}/3$. Whereas, the obtained results with the proposed approach remain the same in variations and amplitude.

Figure 7 THDs comparison (see online version for colours)

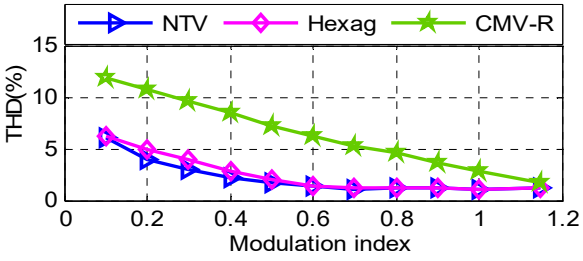
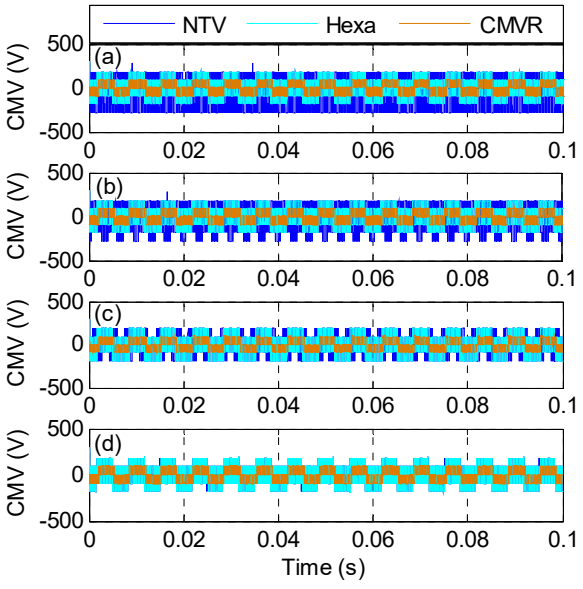


Figure 8 Obtained CMV waveforms for, (a) $m = 0.4$ (b) $m = 0.6$ (c) $m = 0.8$ (d) $m = 1.15$ (see online version for colours)



For further demonstration, the frequency domain waveforms of the obtained CMVs is analysed and depicted in Figure 9 for different values of m. As it is observed from Table 3, the most crucial low-frequency harmonics in CMV are obtained with both conventional methods and they are located around the switching frequency (5 Khz). For the NTV method, they are equal to 166.9 V, 160.7 V, 130.5 V and 49.9 V for the values of $m = 0.4$, $m = 0.6$, $m = 0.8$ and $m = 1.15$, respectively. While, for the hexagon method, they are equal to 111.6 V, 129.6 V, 122.8 V and 49.9 V for $m = 0.4$, $m = 0.6$, $m = 0.8$ and $m = 1.15$, respectively. In the counterparty, with the proposed algorithm, they are decreased to 7.3 V, 20.5 V, 24.2 V and 7.4 V for $m = 0.4$, $m = 0.6$, $m = 0.8$ and $m = 1.15$, respectively.

Figure 9 Frequency spectra of CMV, (a) $m = 0.4$ (b) $m = 0.6$ (c) $m = 0.8$ (d) $m = 1.15$ (see online version for colours)

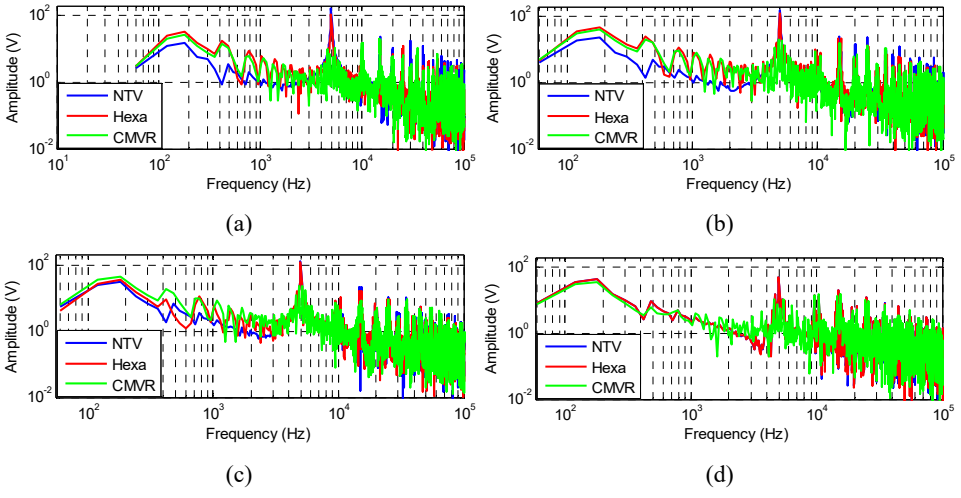


Table 3 The amplitude of the harmonics in the CMV located at the switching frequency

Modulation index m	*NTV-SVM*	*Hexa-SVM*	*CMVR-SVM*
0.4	166.9 V	111.6 V	7.3 V
0.6	160.7 V	129.6 V	20.5 V
0.8	130.5 V	122.8 V	24.2 V
1.15	49.9 V	49.9 V	7.4 V

Figure 10 Obtained I_L waveforms, (a) $m = 0.4$ (b) $m = 0.6$ (c) $m = 0.8$ (d) $m = 1.15$ (see online version for colours)

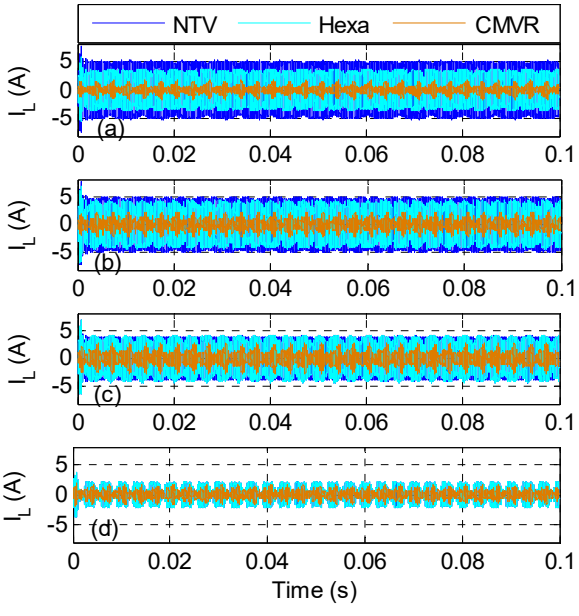


Figure 11 Comparison of RMS of I_L (see online version for colours)

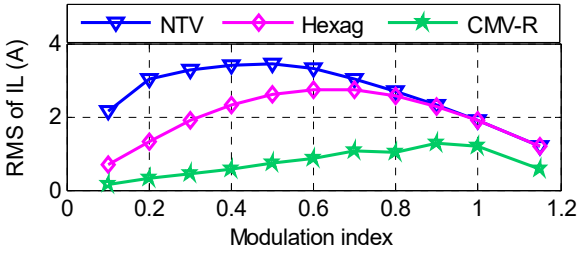


Figure 12 Comparison of the number of commutations of Ka1 and Ka2 (see online version for colours)

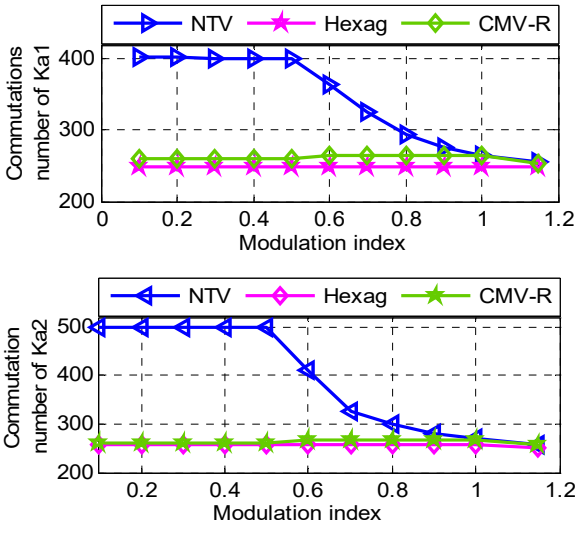


Figure 13 Principle of the hardware co-simulation (see online version for colours)

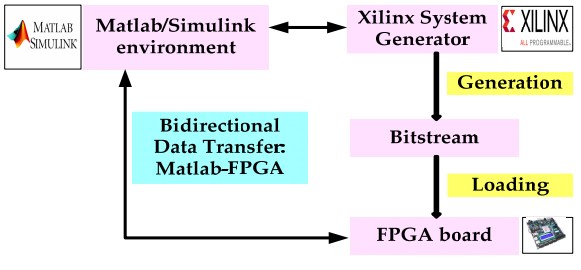


Figure 10 displays the waveforms of the CMC (I_L) acquired using both traditional SVMs and the newly suggested algorithm. It is evident that the conventional SVMs result in a substantial leakage current for the different values of m. Furthermore, for low values of m, it can be noted that the NTV approach produces the highest leakage current since it generates the highest variations and amplitude of CMV. Moreover, for high values of m, the two traditional methods have similar results. The results illustrated in Figure 11

underscore this analysis. The most important RMS values of I_L are effectively produced by both traditional methods. As for the proposed algorithm, it offers a considerable attenuation in the RMS of I_L. Also, the proposed algorithm is evaluated in terms of switching losses when the number of commutations of the two upper power devices of the first phase are computed. The obtained result is shown in Figure 12 when it is compared with the ones produced by the conventional approaches. It can be seen that the proposed algorithm provides similar results with the hexagon method since they treat the reference voltage with the same procedure. The conventional NTV algorithm yields the maximum number of commutations, indicating that it results in the highest switching losses.

5.2 Real-time implementation using XSG Blockset

The hardware co-simulation test is essential to determine the appropriate precision for various XSG blocks and to verify the proper functioning of the proposed algorithm. However, it is important to note that certain functions, like trigonometric functions, may not be readily accessible in the Xilinx toolboxes. In these situations, it becomes necessary to create custom blocks using the existing components within XSG to replicate the functionality of the desired Simulink blocks. In our work, the unavailable blocks are programmed and generated using a fixed-point format, allowing for the selection of both the range and precision of each required block. Each parameter of the XSG block must be carefully considered. This includes selecting parameters that ensure high computational accuracy while also providing fast execution through the parallel processing capabilities of FPGA chips. One of the most critical parameters is the configuration of the input-output register for each XSG function, which relies on the counter blocks. In our work, the execution period is set to the clock frequency of the adopted FPGA, which is set to 10 ns. Additionally, the sampling time for the XSG simulation is fixed at 1 µs. The principle of the hardware co-simulation is presented in Figure 14. Also, an example of the XSG blocks of the proposed SVM algorithm is depicted in Figure 14.

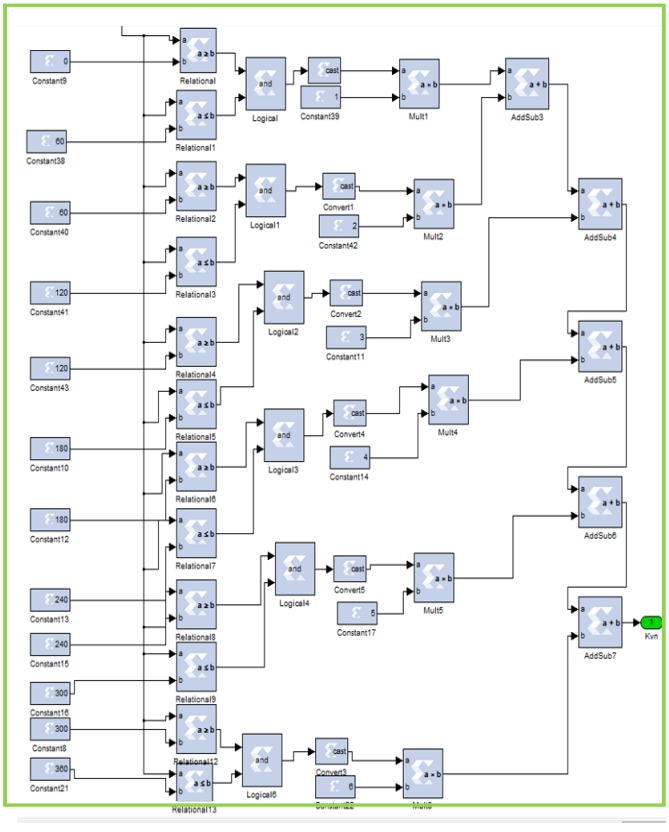
The analysis of system performance is carried out using identical parameters to those employed in the software tests. The acquired results, as illustrated in Figure 15, show high performance of the proposed SVM approach for IM control under steady-state operation with CMV and leakage current reduction.

6 Conclusions

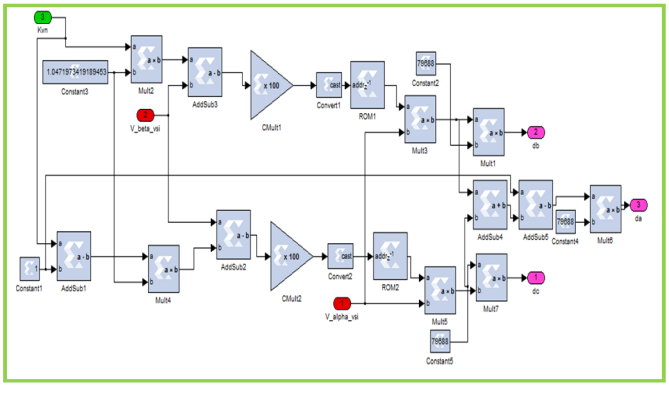
In this paper, we suggested a novel SVM scheme that reduces the CMV and the CMC in 3L NPC inverter fed IM dedicated to PVP systems. The suggested approach mitigated the CMV effects of the conventional SVM algorithms using a virtual approach to synthesise the zero voltage vector. The obtained software and hardware results have exhibited an improved performance in terms of CMV and CMC with reduced complexity, low computation burden and high DC-bus utilisation ratio. The hardware implementation of the proposed algorithm proved its experimental feasibility and optimised the duration of the experimental tests. Adopting the proposed SVM approach with CMV reduction for PVP systems leads to reduced CMC and hence eliminating safety problems. Also, reducing the CMV can extend the lifespan of PV panels and electronic components by

reducing stress and premature failures, leading to improved performance of the overall PVP system.

Figure 14 XSG modelling of, (a) subsector number (b) duty cycles determination (see online version for colours)

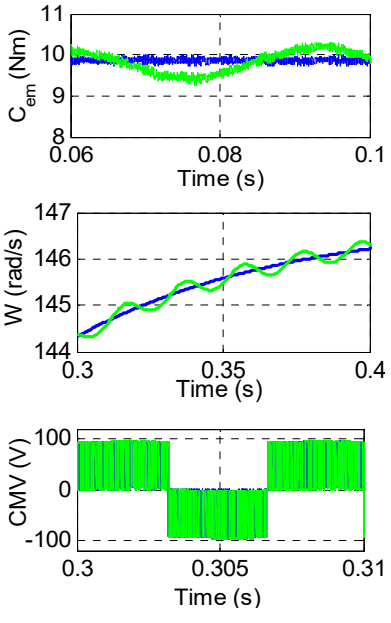


(a)



(b)

Figure 15 Real-time implementation results (blue) software results (green) hardware results (see online version for colours)



As future research avenues, we hope connecting the PV panel with the studied PVP conversion system to evaluate the dynamic of the overall PVP platform. Also, the potential scope entails examining the IM under closed-loop control with a reduced CMV across various speed ranges and torque levels with the aims to assess the effectiveness of the developed control algorithm under different operating conditions.

References

Boussaada, M., Abdelati, R., Lahdhiri, H. and Yahia, H. (2023) 'PV characterization and MPPT based on characteristic impedance using Arduino board and MATLAB interface', *Studies in Informatics and Control*, Vol. 32, No. 1, pp.91–100.

Cavalcanti, M.C., Farias, A.M., Oliveira, K.C. et al. (2012) 'Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems', *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp.435–443.

Chinthamalla, R., Sahoo, D. and Jain, S. (2016) 'A discontinuous switching technique to eliminate common mode voltage with reduced switching losses for an open end winding induction motor drive solar water pump', *IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*, Bhopal, India, pp.1–5.

Guo, F., Yang, T., Diab, A.M., Yeoh, S.S., Bozhko, S. and Wheeler, P. (2021) 'An enhanced virtual space vector modulation scheme of three-level NPC converters for more-electric-aircraft applications', *IEEE Transactions on Industry Applications*, Vol. 57, No. 5, pp.5239–5251.

Hava, A.M. and Ün, E. (2011) 'A high-performance PWM algorithm for common mode voltage reduction in three-phase voltage source inverters', *IEEE Trans. Power Electron.*, Vol. 26, No. 7, pp.1998–2008.

Huang, J. and Li, K. (2020) 'Suppression of common-mode voltage spectral peaks by using rotation reverse carriers in sinusoidal pulse width modulation three-phase inverters with CFM', *IET Power Electron.*, Vol. 13, No. 6, pp.1246–1256.

Jain, S. et al. (2023) 'High-performance hybrid MPPT algorithm based single-stage solar PV fed induction motor drive for standalone pump application', *IEEE Transactions on Industry Applications*, Vol. 59, No. 6, pp.7103–7115.

Jiang, W., Wang, P., Ma, M., Wang, J., Li, J., Li, L. and Chen, K. (2020) 'A novel virtual space vector modulation with reduced common-mode voltage and eliminated neutral point voltage oscillation for neutral point clamped three-level inverter', *IEEE Trans. Ind. Electron.*, Vol. 67, No. 2, pp.884–894.

Mahmoud, Z., Hamouda, M. and Khedher, A. (2017a) 'Space vector modulation of multilevel inverters: a simple and fast method of two-level hexagon's selection', *Int. J. Power Electron*., Vol. 8, No. 2, pp.107–123.

Mahmoud, Z., Hamouda, M. and Khedher, A. (2017b) 'A comparative study between the nearest three vectors and two-level hexagons based space vector modulation algorithms for three-level NPC inverters', *International Journal of Renewable Energy Research*, Vol. 7, No. 3, pp.1074–1084.

Mahmoud, Z., Hamouda, M. and Khedher, A. (2019) 'Direct power control with common mode voltage reduction of grid-connected three-level NPC inverter', *IET Power Electronics*, Vol. 12, No. 3, pp.400–409.

Mansuri, A., Maurya, R. and Suhel, S.M. (2023) 'Reduction of common-mode voltage using zero voltage vectors in dual star asymmetrical induction motor', *IEEE Transactions on Energy Conversion*, Vol. 38, No. 1, pp.230–238.

Mittal, N., Singh, B., Singh, S.P., Dixit, R. and Kumar, D. (2012) 'Multilevel inverters: a literature survey on topologies and control strategies', in *Proc. 2nd Int. Conf. Power, Control Embedded Syst.*, pp.1–11.

Nabae, A., Takahashi, I. and Akagi, H. (1981) 'A new neutral-point-clamped PWM inverter', *IEEE Trans. Ind. Appl.*, Vol. IA-17, No. 5, pp.518–523.

Qin, C., Zhang, C., Xing, X., Li, X., Chen, A. and Zhang, G. (2020) 'Simultaneous common-mode voltage reduction and neutral-point voltage balance scheme for the quasi-Z-source three-level T-type inverter', *IEEE Transactions on Industrial Electronics*, Vol. 67, No. 3, pp.1956–1967.

Rao, M.N., Karthick, N. and Rao, A.M. (2022) 'Energy balancing capability of a three phase nine-level inverter for solar water pumping applications', *International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC)*, Mathura, India, pp.1–6.

Saoudi, A., Krim, S. and Mimouni, M.F. (2021) 'Enhanced intelligent closed loop direct torque and flux control of induction motor for standalone photovoltaic water pumping system', *Energies*, Vol. 14, No. 24, p.8245.

Singh, B. and Kumar, R. (2016) 'Simple brushless DC motor drive for solar photovoltaic array fed water pumping system', *IET Power Electron.*, Vol. 9, No. 7, pp.1487–1495.

Sonak, S. and Bhim, S. (2015) 'Solar PV water pumping system with DC-link voltage regulation', *International Journal of Power Electronics*, Vol. 7, Nos. 1/2, pp.72–85.

Sunil Kumar, G. and Rajan, K. (2023) 'Synchronization of solar PV-wind-battery-based water pumping system using brushless DC motor drive', *International Journal of Power Electronics*, Vol. 18, No. 4, pp.435–459.

Zarrad, O., Hajjaj, M.A. and Mansouri, M.N. (2019) 'Hardware implementation of hybrid wind-solar energy system for pumping water based on artificial neural network controller', *Studies in Informatics and Control*, Vol. 28, No. 1, pp.35–44.

Appendix

IM parameters

Rated power	1.5 kW
Rated speed	1,435 r/min
Rated frequency	50 Hz
Rated current	5.5/3.2 A
Number of pole pairs	2
Stator resistance	5.72 Ω
Rotor resistance	4.28 Ω
Stator inductance	0.464 H
Rotor inductance	0.464 H
Mutual inductance	0.44 H
Moment of inertia	0.0049 kg.m^2
Viscous friction coefficient	0.002