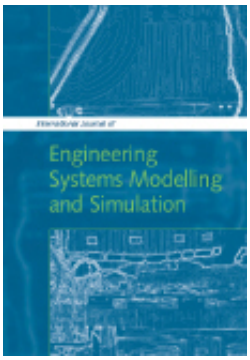


International Journal of Engineering Systems Modelling and Simulation

ISSN online: 1755-9766 - ISSN print: 1755-9758
https://www.inderscience.com/ijesms

Hysteresis controlled single phase-VIENNA rectifier fed DC drive system with enhanced response

B. Manimaran, R. Rani Hemamalini, Ramareddy Sathi

DOI: 10.1504/IJESMS.2022.10046834

Article History:
Received: 17 September 2021
Accepted: 28 January 2022
Published online: 01 December 2023

Hysteresis controlled single phase-VIENNA rectifier fed DC drive system with enhanced response

B. Manimaran* and R. Rani Hemamalini

Department of Electrical and Electronics Engineering,
St. Peter's Institute of Higher Education and Research,
Tamil Nadu, India
Email: manimaran.b@ritchennai.edu.in
Email: ranihema1@yahoo.com
*Corresponding author

Ramareddy Sathi

Department of Electrical and Electronics Engineering,
Rajalakshmi Engineering College,
Chennai, India
Email: ramareddy.s@rajalakshmi.edu.in

Abstract: This work deals with the forming, enquiry, strategy and simulation of proportional resonant-proportional resonant (PR-PR) and hysteretic-controlled two loop single-phase VIENNA rectifier fed DC drive system (SPVRDDS) using MATLAB Simulink. VIENNA rectifier with low THD is proposed for the control of DC drive. HC is suggested for closed loop SPVRDDS. Simulation is done for PR (proportional resonant controller) and PI-HC (proportional integral-hysteresis controller) controlled two loop systems using VIENNA rectifier fed DC drive and the outcomes are evaluated. The assessment is done in terms of time domain parameters like settling time and steady state error. The endings of SPVRDDS represent grander concert of HC controlled two loops VIENNA.

Keywords: THD; PIC; PRC; Swiss-rectifier; PWM-control.

Reference to this paper should be made as follows: Manimaran, B., Hemamalini, R.R. and Sathi, R. (2024) 'Hysteresis controlled single phase-VIENNA rectifier fed DC drive system with enhanced response', *Int. J. Engineering Systems Modelling and Simulation*, Vol. 15, No. 1, pp.27–36.

Biographical notes: B. Manimaran is a research scholar at the Department of Electrical and Electronics Engineering, St. Peter's Institute of Higher Education and Research, Avadi, Chennai. Currently, he is working as an Assistant Professor at the Department of Electrical and Electronics Engineering, Rajalakshmi Institute of Technology, Chennai and he is serving in the field of teaching for the past ten years.

R. Rani Hemamalini is serving in the field of teaching for the past 27 years at various levels. Currently, she is working as a Professor and the Head of the Department of Electrical and Electronics Engineering and also IQAC Coordinator at St. Peter's Institute of Higher Education and Research, Avadi, Chennai. Her area of research includes process controls and instrumentation, embedded system and VLSI.

Ramareddy Sathi is a Professor of Electrical Department, Rajalakshmi Engi- neering College, Chennai. He obtained his DEE from S.M.V.M Polytechnic, Tanuku, A.P., A.M.I.E in Electrical Engineering from the Institution of Engineers, India and ME in Power System Anna University. He received his PhD degree in the area of Resonant Converters from College of Engineering, Anna University, Chennai.

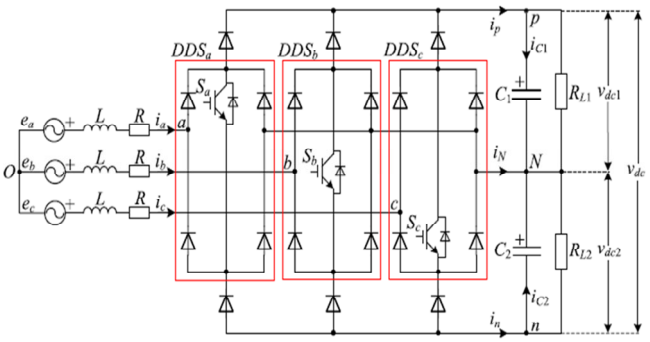
1 Introduction

Starting late, VIENNA rectifier (Kolar and Zach, 1997; Minibock and Kolar, 2005) had pulled in an ever-expanding number of contemplations as well as relate to various circumstances owing to its wonderful pieces. For the moment, extraordinary-control frameworks for VIENNA rectifier had been intended. The circuit topography of VIENNA rectifier is showed up in Figure 1. In Maswood et al. (2011), the hysteresis current control (HCC*) system had been related to govern the-VIENNA rectifier. *HCC had various positive conditions, for instance, fast incredible

response, extraordinary energy, etc. In any case, the HCC had its peculiar burdens-too, exclusively-when-it was grasped to govern the 3phase-converters. For instance, it can't take out the coupling among the 3phase streams which realises extended trading state trading-number in addition to-current-harmonics.

The current following mistake will outperform two fold-the hysteresis transfer speed limit (Mohseni and Islam, 2010). In Wei et al. (2014) and Gao et al. (2017), the 1cycle govern method was grasped to govern the VIENNA rectifier, and a brisk one of a kind response had been cultivated. In any case, 1cycle control method was generally executed with straightforward mode which will realise a troublesome change strategy of boundaries. In Hang et al. (2014) and Markkandan et al. (2021b), the vector-control system reliant on SV-PWM was grasped to the govern method of-VIENNA rectifier. The PI estimation was direct and full developed, anyway as broadly known, it was fragile to structure boundaries and had a deprived ground-breaking display.

Figure 1 Topology of V-R (see online version for colours)



The -SV-PWM computation requisite a ton of count, exclusively while it was cast off in 3level geographies. Starting late, separating the inertia of *VIENNA rectifier then consuming the positive-based control (*PBC) routine to govern *VIENNA rectifier had pulled in an ever-expanding number of contemplations. In Markkandan et al. (2021a), the absence of inclusion of *VIENNA rectifier was examined and the govern hover with *PBC speculation was organised. In any case, the arrangement strategy of PBC controller was to some degree puzzling. Starting late, new technique comprising the gains of equally *HCC and *PI-based-vector-control had-been locked in Leonid and Jayaparvathy (2021).

This technique -can join-the straightforwardness and pace of CH-CC and incredible govern execution of vector govern. Be that as it may, the above strategies, other control philosophies had been investigated too (Thangamani et al., 2020b). These-methodology had their own characteristics. Besides, these philosophies had chance to improve. For instance, improving the philosophies and lessen the reliance on logical -model precision was favourable. In this, the indistinguishable system from 3 level-voltage-vector of *VIENNA rectifier to 2 level voltage-vector was found. By which, 1essential time of *VIENNA rectifier was apportioned in-to 6 areas and each part was controlled as a 3 phase 2 level VSR. Blend with the three-stage VSR, a space-vector exchanging design hysteresis control (*SVSPHC) methodology was intended. The hypothetical deduction of *SVSPHC* was introduced. Then, the usage procedure of guiding VIENNA *rectifier with *SVSPHC* was demonstrated as well.

The beyond-writing does not pact with the speed-guideline of the VIENNA rectifier-DD System with HC regulator. In this, a HC* for the guideline of the V-RDDS is intended.

2 VIENNA rectifier

The principal structure some portion of the VIENNA rectifier is the check of the estimation of the DC-interface capacitor. The advancement proposed for solitary-stage unprejudiced associated VIENNA rectifier and 3 stage VIENNA rectifier are showed up in Figure 2 and Figure 2(a) independently. The 4 techniques for action subject to the current stream and status of the essential switch of 3 phase geography are showed up in Figure 2(b).

a the-line current is certain and the controlled switch is off

b the line current is sure and the controlled-switch is-on

c the line-current is ve and the controlled switch is off

d the line-current is ve and the controlled switch is on.

The incorporated 3l evels AC side voltage affects the rectifier DC side yield circuit structure. Figure 2(c) presents identical-plan of the VIENNA rectifier yield circuits.

Two of the 3streams idc+, idc-and in are free and may be addressed in the DC yield circuits by the current source compelled by the state of force electronic switches. The 3rd current is a tribute of the 2others.

By virtue of sinusoidal guideline, the typical estimations of the idc+ and idc-streams are proportionate to each other and identical to the ordinary estimation of the store current i0 (Equa1).

$$Idc(Ave)+ = Idc-(Ave) = I0(Ave)\ and\ In(Ave) = 0 \quad (1)$$

It infers that the normal estimation of the in current is 0. Consequently, normal estimations of the capacitor voltages are equivalent to one another. On account of huge estimations of the capacitors it might be guaranteed that the quick estimations of the capacitor voltages are almost steady and equivalent to one another.

From the 4operational modes and the proportionate plan of the rectifier which are indicated separately in Figure 2(b) and Figure 2(c), capacitors flows (i_C + and i_C–) are

$$i_C = i_{dc} + i_0 \quad (2)$$

$$i_C = i_{dc} i_0 \quad (3)$$

i.e.

$$in = i_{dc} i_{dc} \quad (4)$$

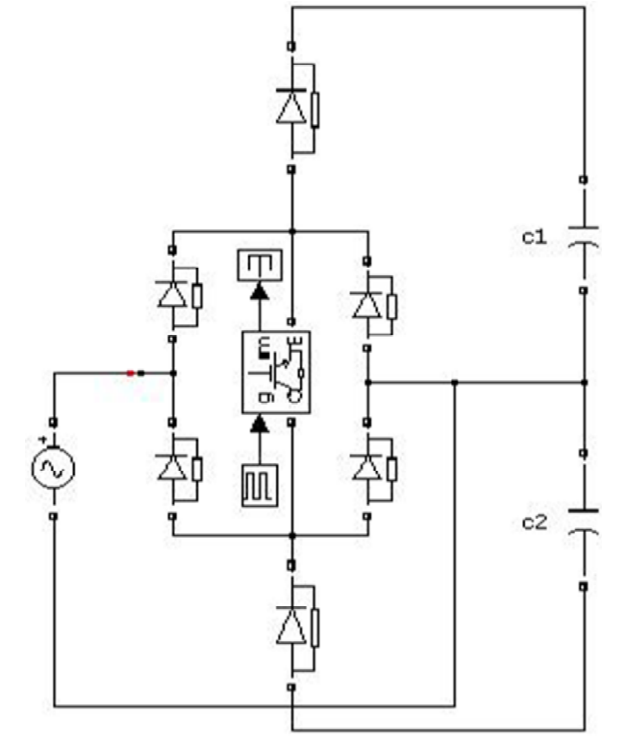
and

$$in = i_C i_{C+} \tag{5}$$

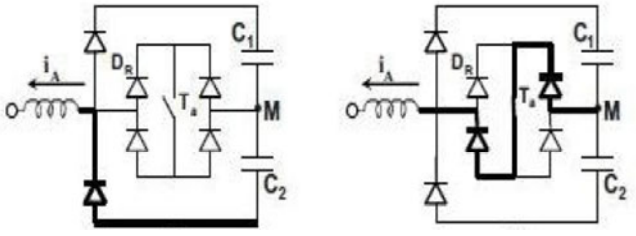
Figure 2(d), the rectifier DC-yield voltage is the aggregate of the capacitor voltages of the yield circuit

$$udc = udc_+ + udc \tag{6}$$

Figure 2 Proposed circuit of a 1phase-neutral-linked VIENNA rectifier, (a) circuit diagram of a 3 phase VIENNA rectifier (b) modes of-operation-based on current-conduction path (c) equivalent scheme of the output circuit of VIENNA rectifier (d) blockschematic of VIENNA rectifier's DC output-circuits (see online version for colours)

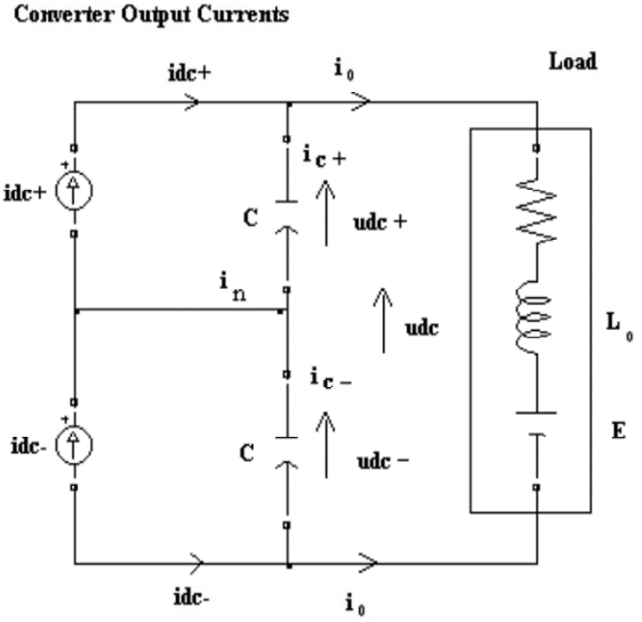


(a)

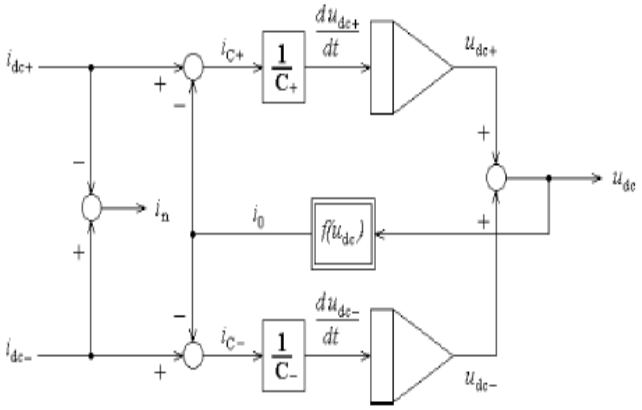


(b)

Figure 2 Proposed circuit of a 1phase-neutral-linked VIENNA rectifier, (a) circuit diagram of a 3 phase VIENNA rectifier (b) modes of-operation-based on current-conduction path (c) equivalent scheme of the output circuit of VIENNA rectifier (d) blockschematic of VIENNA rectifier's DC output-circuits (continued) (see online version for colours)



(c)



(d)

By and large the DC yield current is the non-direct capacity of the rectifier-DC-interface voltage

$$i_0 = f\left(u_{dc}\right) \tag{7}$$

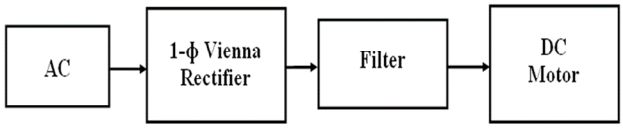
Figure 2(d) speaks to the schematic-graph of the deliberate conditions depicting the VIENNA rectifier DC yield functionality.

The equations of DCM-are as follows:

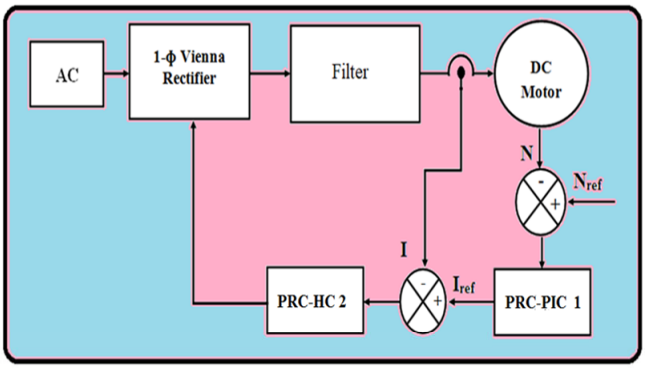
$$Vv = Ri + L\ di/dt + e\ bac \tag{8}$$

$$T = Tl + J\ dw/dt + Bw \tag{9}$$

Figure 3 (a) Block diagram of proposed single phase VIENNA rectifier (b) Simulation block diagram of 2loop SPVR-DDS with PRC/-Hysteresis controllers (see online version for colours)



(a)



(b)

3 System description

Lastly the DC motor fed-from the SPVR is portrayed in the Figure 3(a). Fixed-AC is converted to variable – DC using V.R. The output of V.R. is filtered using split – capacitor filter.

SPVR-DDS with PRC-PRC/PI-HC is portrayed in Figure 3(b). The-speediness of-DCM is narrated with a – refer-speediness. The flaw is sensible to the speediness – PRC-PRC/PI-HC. The yields fPRC-PRC/PI-HC is applied as the current-reference. The Irefis evaluated with the authentic-current* to get *current-slip. The flaw is pragmatic to the current-PRC-PRC/PI-HC. The comparator apprises the pulse-width intended to VR.

4 Results and discussion

4.1 Open loop SPVRDDS with source disturbance

Figure 4 delineates the circuit diagram of open loop VIENNA rectifier with source disturbance. Figure 5 delineates the input voltage prearranged to the method. The input voltage value is increased from 48V to 55V. Figure 6 delineates the Voltage across motor load with source-disturbance. The value of Voltage across motor load increases and reaches value of 150V. Figure 7 delineates the Motor speed with source-disturbance. The value of motor speed increases and reaches steady state with the value of 1700 RPM. Figure 8 delineates the Current through motor load with source-disturbance. The value of Current through motor load initially increases and then decreases with the value of 13A. Figure 9 delineates the Motor torque with source-disturbance and the value attained is 7N-m.

Figure 4 Circuit diagram of open loop SPVRDDS with source disturbance (see online version for colours)

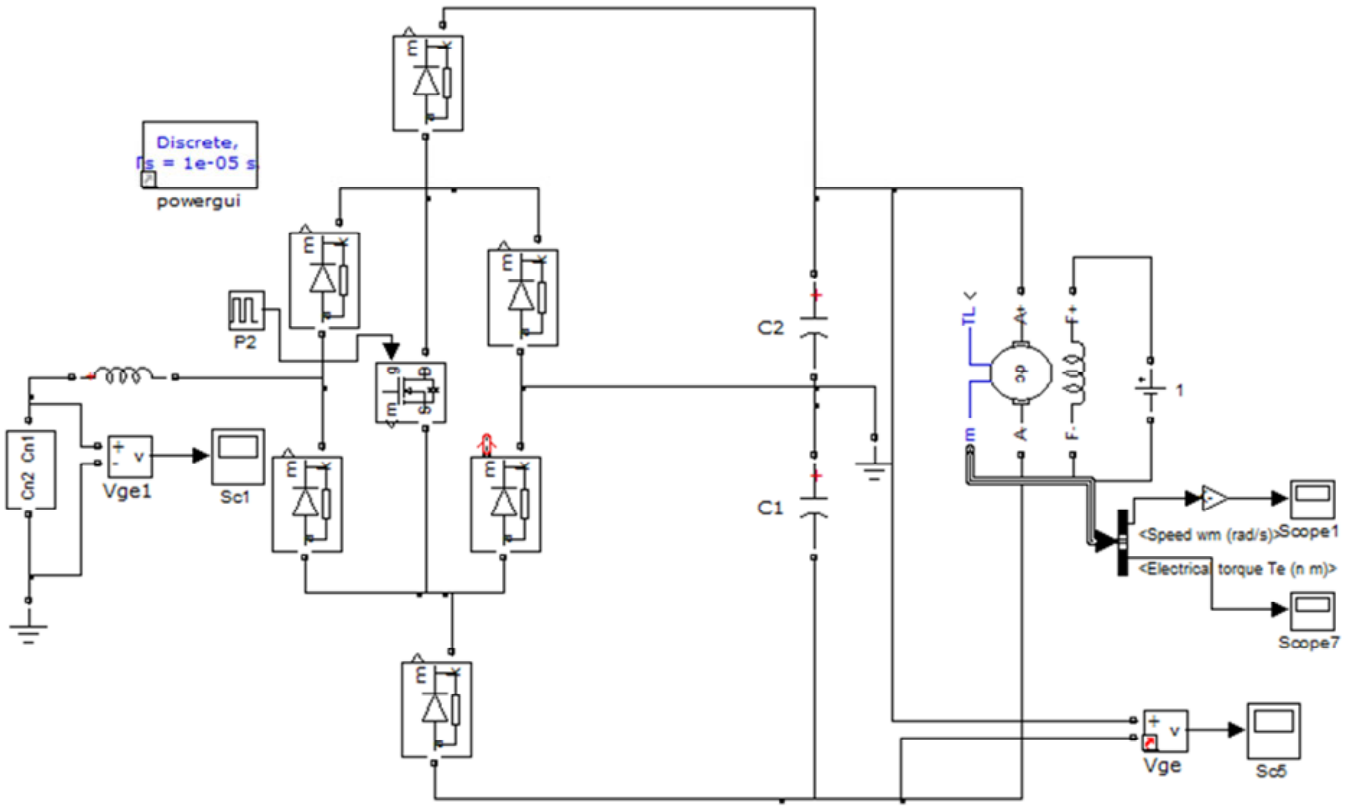


Figure 5 Input voltage of open loop SPVRDDS with source disturbance (see online version for colours)

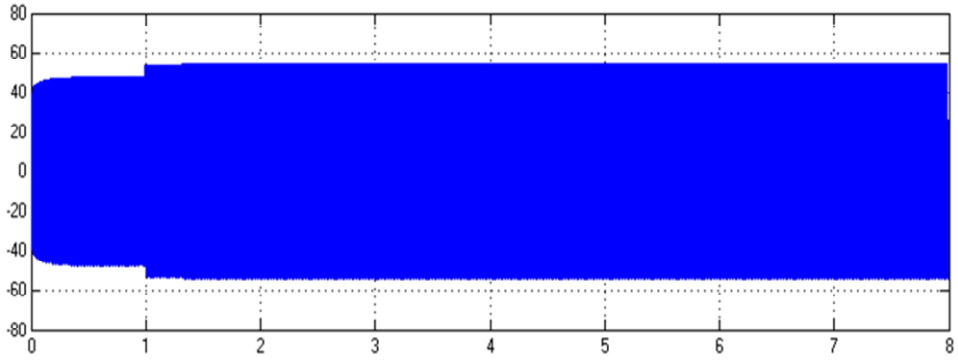


Figure 6 Voltage across motor load of open loop SPVRDDS with source disturbance (see online version for colours)

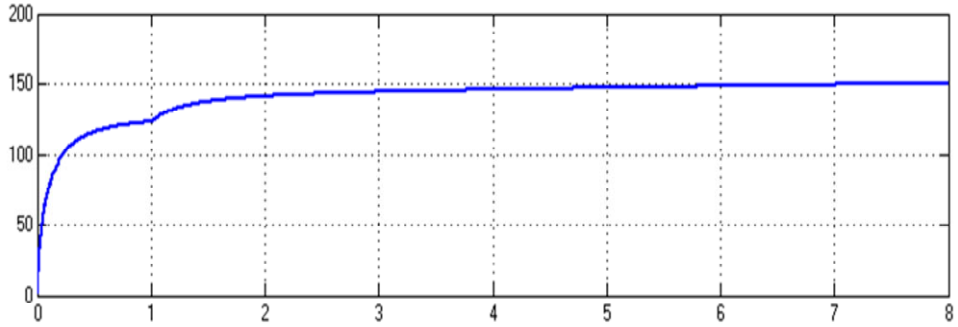


Figure 7 Motor speed of open loop SPVRDDS with source disturbance (see online version for colours)

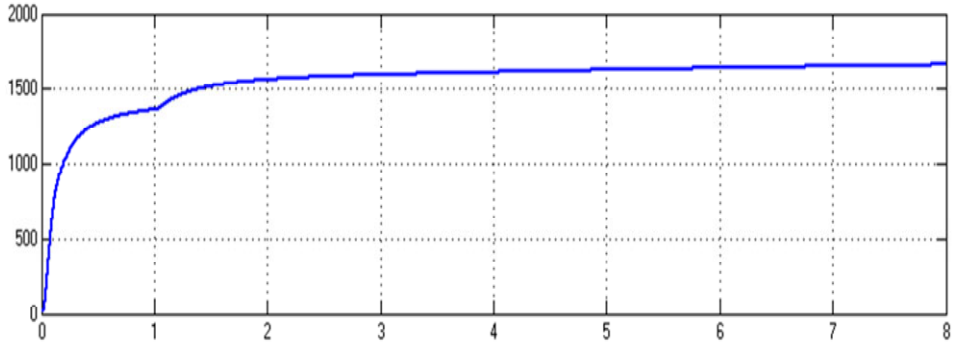


Figure 8 Current through motor load of open loop SPVRDDS with source disturbance (see online version for colours)

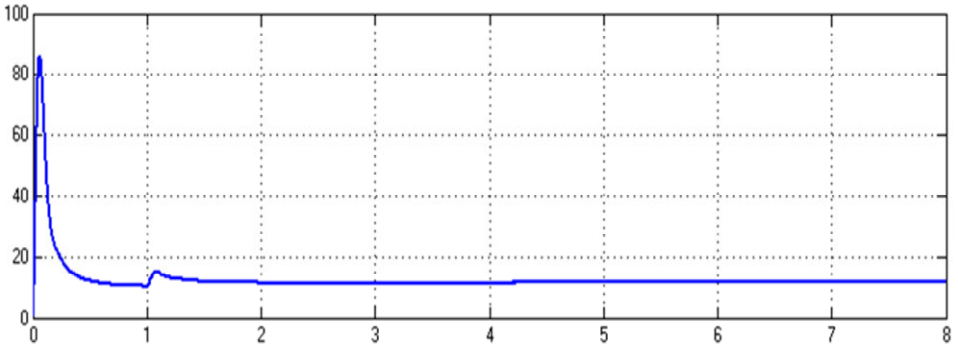


Figure 9 Motor torque of open loop SPVRDDS with source disturbance (see online version for colours)

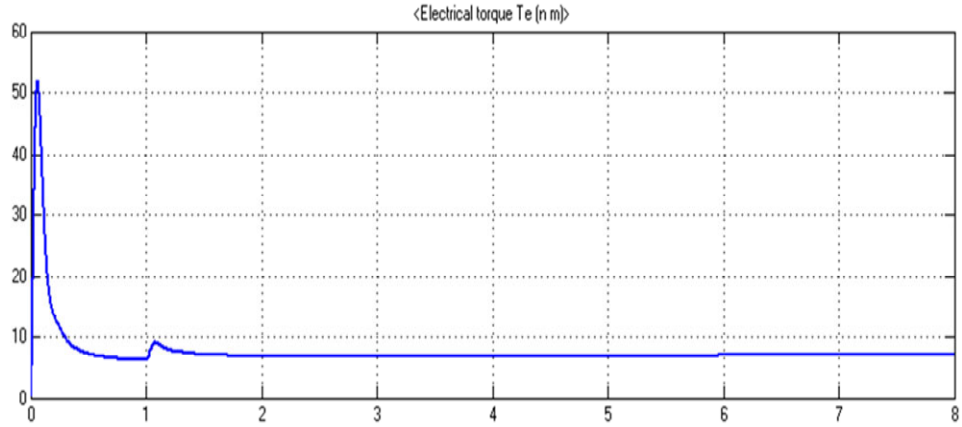
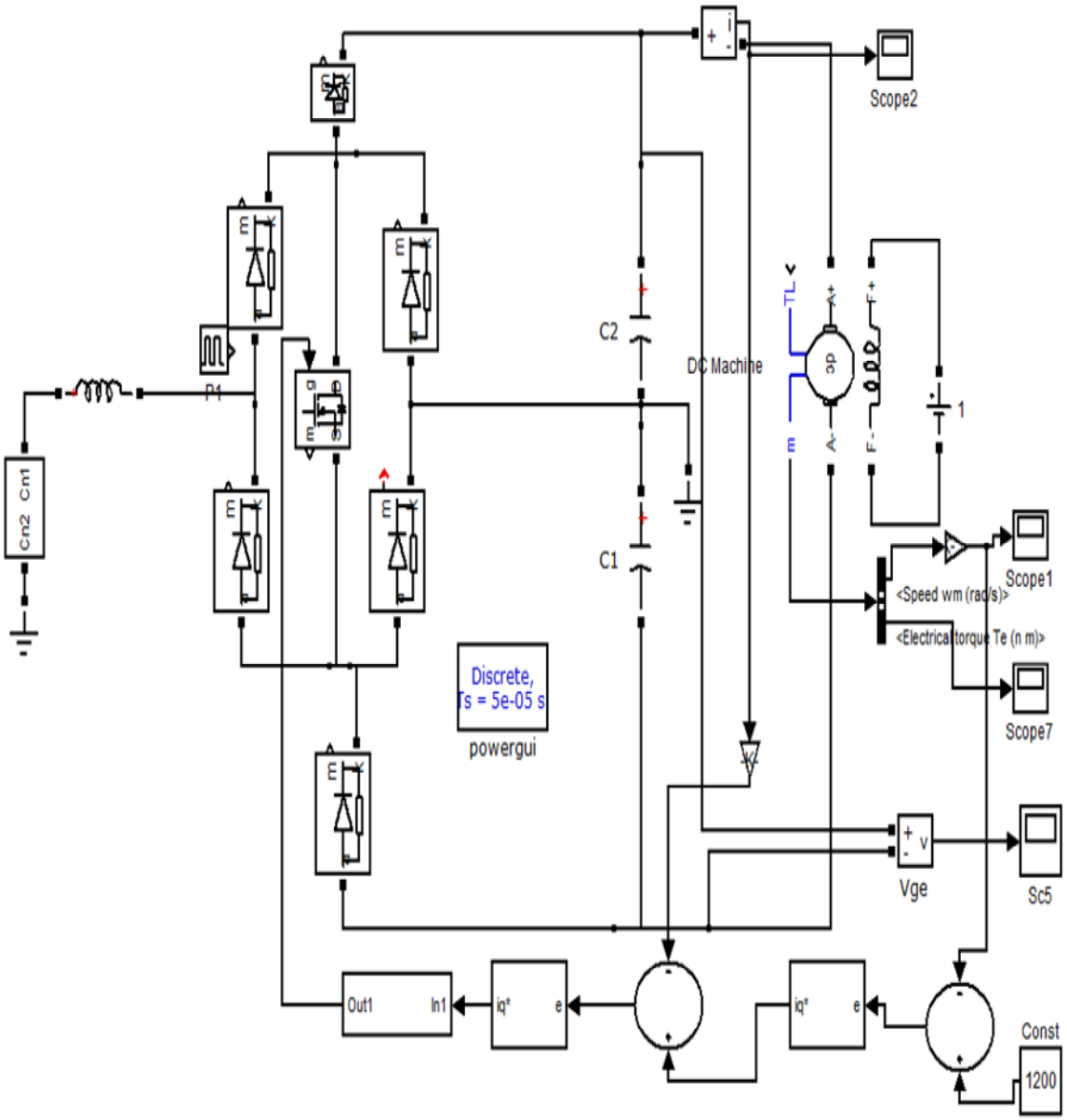


Figure 10 Two loop SPVRDDS with PR-PR controller (see online version for colours)



4.2 Two loop SPVRDDS with PR-PR controller

Figure 10 delineates the circuit diagram of two loop VIENNA rectifier with PR-PR controller. The comparator apprises the pulse-width applied to VR.

Figure 11 delineates the input voltage given to the system. The input voltage value is increased from 48V to 55V. Figure 12 delineates the voltage across motor load. The value of Voltage across motor load gradually decreases and reaches steady state with the value of 110V. Figure 13 delineates the Motor speed. The value of motor speed gradually decreases and reaches steady state with the value of 1250 RPM. Figure 14 delineates the Current through motor load. The value of Current through motor load is 10 A. Figure 15 delineates the Motor torque and the value attained is 5 N-m.

Figure 11 Input voltage of two loop SPVRDDS with PR-PR controller (see online version for colours)

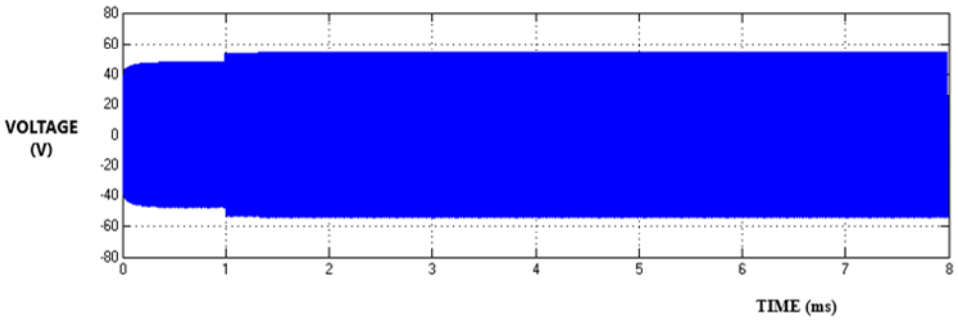


Figure 12 Voltage across motor load of two loop SPVRDDS with PR-PR controller (see online version for colours)

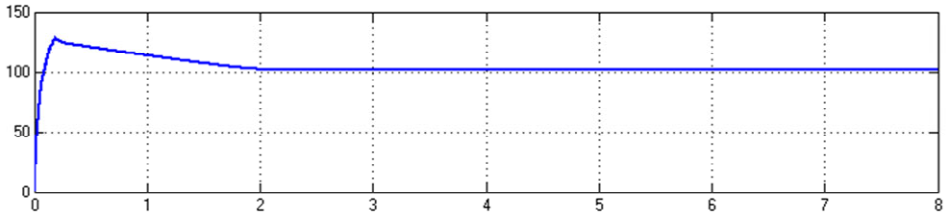


Figure 13 Motor speed of two loop SPVRDDS with PR-PR controller (see online version for colours)

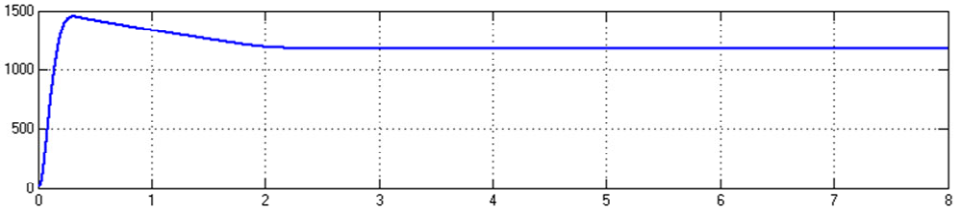


Figure 14 Current through motor load of two loop SPVRDDS with PR-PR controller (see online version for colours)

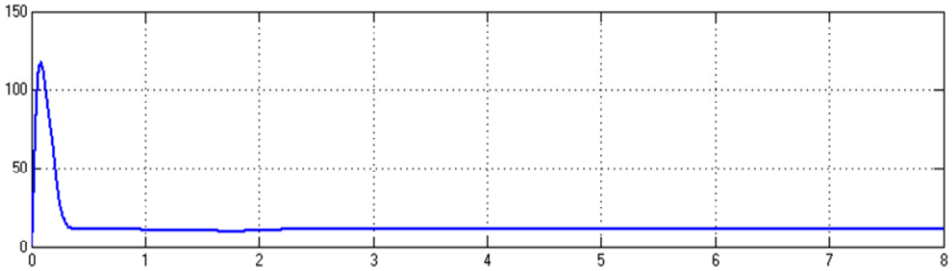


Figure 15 Motor torque of two loop SPVRDDS with PR-PR controller (see online version for colours)

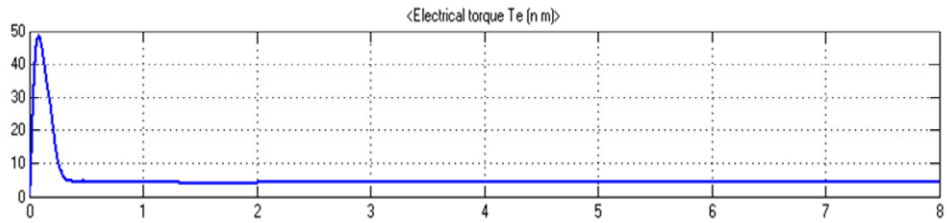


Figure 16 Circuit diagram of two loop SPVRDDS with HC controller (see online version for colours)

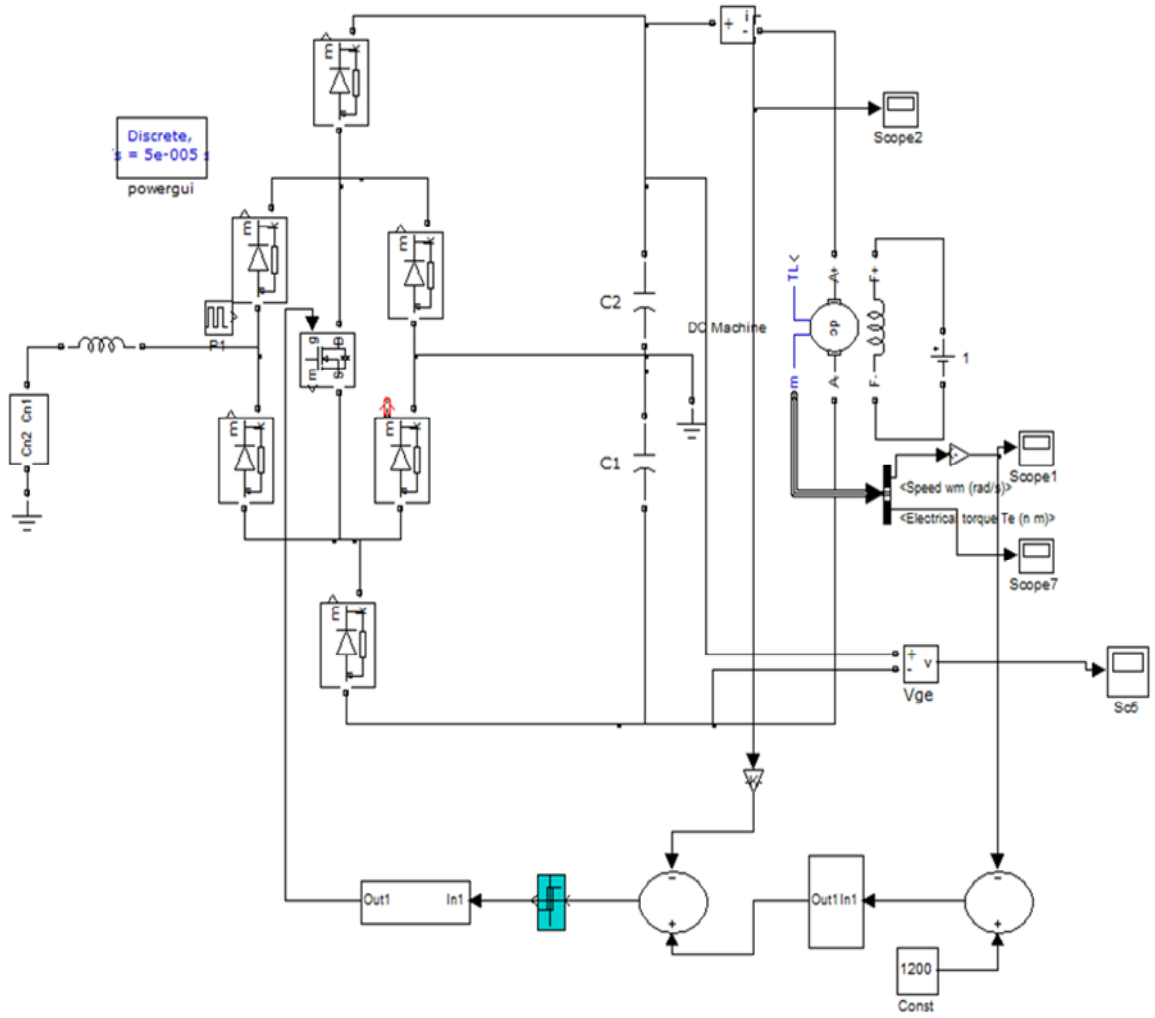


Figure 17 Input voltage of two loop SPVRDDS with HC controller (see online version for colours)

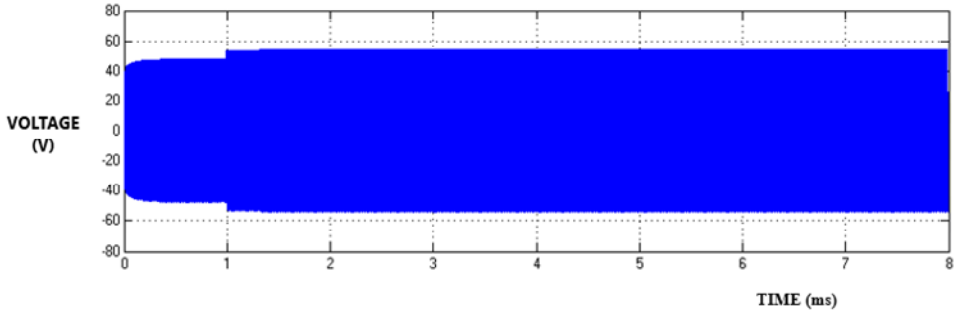


Figure 18 Voltage across motor load of two loop SPVRDDS with HC controller (see online version for colours)

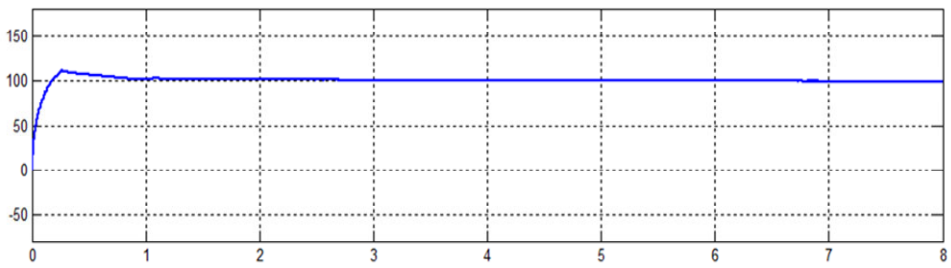


Figure 19 Motor speed of two loop SPVRDDS with HC controller (see online version for colours)

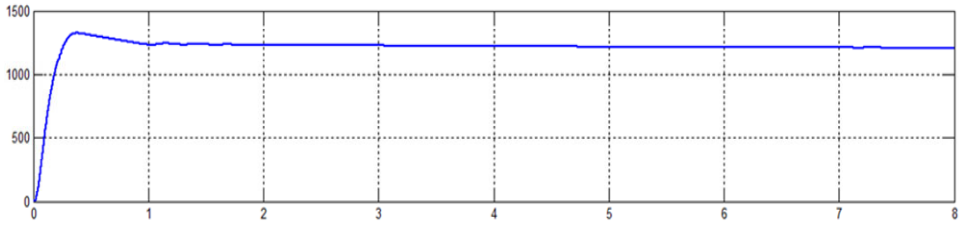


Figure 20 Current through motor load of two loop SPVRDDS with HC controller (see online version for colours)

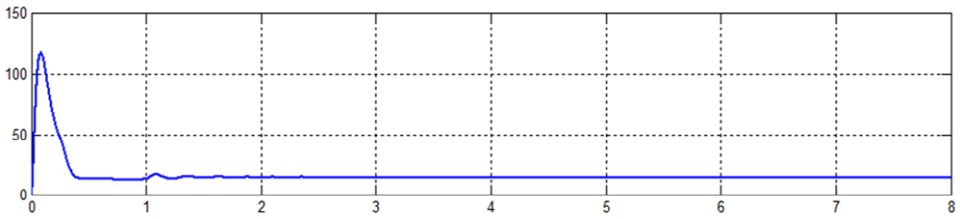
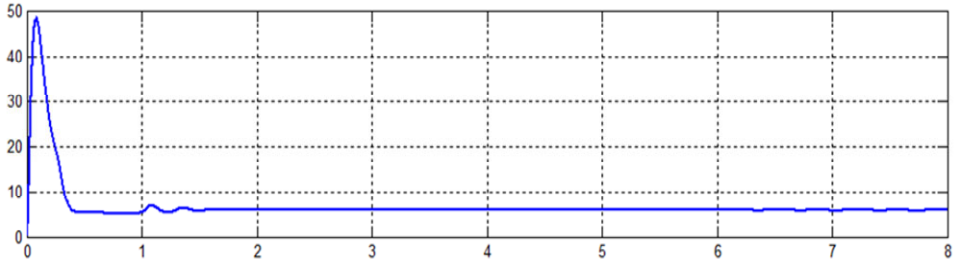


Figure 21 Motor torque of two loop SPVRDDS with HC controller (see online version for colours)

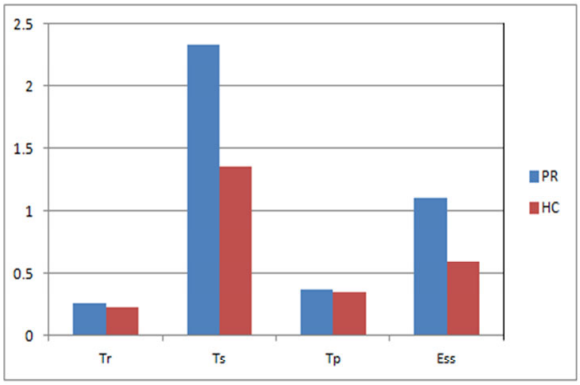


4.3 Two loop SPVRDDS with HC- controller

Figure 16 delineates the circuit diagram of two loop VIENNA rectifier with -HC controller. Figure 17 delineates the input voltage given to the system. The input voltage value is increased from 48V to 55V. Figure 18 delineates the voltage across motor load with -HC controller. The value of Voltage across motor load gradually decreases and reaches steady state with the value of 100V. Figure 19 delineates the motor speed with -HC controller. The value of motor speed decreases and reaches steady state quickly with the value of 1250 RPM. Figure 20 delineates the Current through motor load with -HC controller. The value of Current through motor load is 10 A. Figure 21 delineates the Motor torque with -HC controller and the value attained is 6 N-m.

Comparison of time domain parameters using PR-PR and PI-HC are given in Table-1.By using PI-HC, the risetime is reduced from 0.26 Sec to 0.23Sec; peak time is reduced from 0.37 Sec to 0.35 Sec; settling time is reduced from 2.33 Sec to 1.35 Sec; steady state error is reduced from 1.1 V to 0.6 V. Figure 22 outlines the bar chart representation of time domain parameters using PR-PR and PI-HC. Hence, the outcome represents that the PI-HC controlled two-loop VIENNA rectifier superior to PR-PR controlled two loop VIENNA rectifier.

Figure 22 Bar chart comparison of time domain parameters using PR-PR and PI-HC (see online version for colours)



5 Conclusions

Open loop and two loop VIENNA rectifier with PR-PR(proportional resonant) controller and PI-HC (proportional integral – Hysteresis controller) are simulated and the outcomes are presented. The endings are related in terms of *settling time &steady state error*. By-using PI-HC, the risetime is reduced from 0.26 Sec to 0.23Sec; peak time is reduced from 0.37 Sec to 0.35 Sec; settling time is reduced from 2.33 Sec to 1.35 Sec; steady state error is reduced from 1.1 V to 0.6 V. Figure 22 outlines the bar chart representation of time domain parameters using

PR-PR and PI-HC. Hence, the outcome represents that the PI-HC controlled two loop VIENNA rectifiers superior to PR-PR controlled two loop VIENNA rectifier. The advantage of SPVRDDS is the requirement of single-switch. The disadvantage of SPVR-DDS is the requirement of larger no. of diodes. The contribution is to augment the time response of SPVRDDS using HC.

Table 1 Comparison of time domain parameters using PR-PR and PI-HC

Controller	**Tr (sec)**	**Ts (sec)**	**Tp (sec)**	**Ess (V)**
PR-PR	0.26	2.33	0.37	1.1
PI-HC	0.23	1.35	0.35	0.6

The present work deals with the simulation of two loop VIENNA rectifier with PR-PR(proportional resonant) controller and PI-HC (proportional integral – Hysteresis controller). FLC-FL controlled two loop VIENNA rectifier can be done in Future.

References

Gao, T., Zhang, S., Zhang, S. and Zhao, J. (2017) 'A dynamic model and modified one-cycle control of three-level front end rectier for neutral point voltage balance', *IEEE Access*, Vol. 5, No. 3, pp.2000–2010.

Hang, L., Li, B., Zhang, M., Wang, Y., Tolbert, L.M. (2014) 'Equivalence of SVM and carrier-based PWM in three-phase/wire/level-VIENNA rectifier and capability of unbalanced load control', *IEEE Trans.-I.El.*, January, Vol. 61, No. 1, pp.20–28.

Kolar, W. and Zach, F.C. (1997) 'A-novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules', *IEEE Trans. I. El.*, August, Vol. 44, No. 4, pp.456–467.

Leonid, T.T. and Jayaparvathy, R. (2021) 'Statistical-model based voice activity identification for human-elephant conflict mitigation', *J. Ambient Intell. Human Comput.*, Vol. 12, pp.5269–5275, https://doi.org/10.1007/s12652-020-02005-y.

Markkandan, S., Malarvizhi, C., Raja, L., Kalloor, J., Karthi, J. and Atla, R. (2021a) 'Highly compact sized circular microstrip patch antenna with partial ground for biomedical applications', *Materials Today: Proceedings*, Vol. 47, Part 1, pp.318–320.

Markkandan, S., Narayanan, L., Robert Theivadas, J. and Suresh, P. (2021b) 'Edge based interpolation with refinement algorithm using EDGE strength filter for digital camera images', *Turkish Journal of Physiotherapy and Rehabilitation*, Vol. 32, No. 2, pp.981–993.

Maswood, A.I., Al-Ammar, E. and Liu, F. (2011) 'Average and hysteresis current controlled three-phase three-level unity power factor rectifier operation and performance', *IET PEl.*, Vol. 4, No. 7, p.752.

Minibock, J. and Kolar, J.W. (2005) 'Novel-concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers', *IEEE Trans. I. Ele.*, February, Vol. 52, No. 1, pp.162–170.

Mohseni, M. and Islam, S.M. (2010) 'A new vector-based hysteresis current control scheme for three-phase PWM voltage source inverters', *IEEE Trans. P. Electron.*, September, Vol. 25, No. 9, pp.2299–2309.

Suresh, P., Saravanakumar, U., Iwendi, C., Mohan, S. and Srivastav, G. (2020) 'Field-programmable gate arrays with low power vision system using dynamic switching', *Computers & Electrical Engineering*, Vol. 90, No. 13, pp.106–996.

Thangamani, M., Vijayalakshmi, R., Ganthimathi, M., Rajita, Malarkodi, P. and Nallusamy, S. (2020b) 'Efficient classification of heart disease using K-Means clustering algorithm', *International Journal of Engineering Trends and Technology*, December, Vol. 68, No. 12, pp.48–53.

Wei, Z., Chen, J., Chen, X., Gong, C.Y., Fan, Y., Chen, J-W. (2014) 'Modiedone cycle controlled three-phase pulse-width modulation rectifiers with a reduced switching frequency to power-line frequency ratio', *IET-P. Electron.*, March, Vol. 7, No. 3, pp.567–575.