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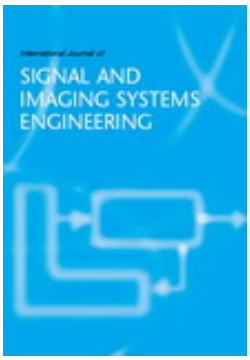

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B. Jaya Lakshmi, R. Ramana Reddy, Naresh K. Darimireddy

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Design of high speed and low power multiplier using dual-mode square adder

B. Jaya Lakshmi*

Department of ECE,
Lendi Institute of Engineering and Technology,
Vizianagaram, Andhra Pradesh, India
Email: jayabobbara04@gmail.com
*Corresponding author

R. Ramana Reddy

Department of ECE,
JNTUA College of Engineering,
Pulivendula, Kadapa, Andhrapradesh, India
Email: profrrreddy@yahoo.com

Naresh K. Darimireddy

Department of ECE,
Lendi Institute of Engineering and Technology,
Vizianagaram, Andhra Pradesh, India
Email: yosuna@ieee.org

Abstract: Adders are the basic building blocks in analogue and digital circuits for implementing arithmetic operations. Different adder designs are reported to obtain high speed, less area and low power dissipation. Dual mode logic (DML) and dual mode addition (DMADD) techniques can be used to achieve low power and high speed addition. Adders are the main blocks in multipliers. In this paper Braun multiplier is implemented using dual-mode (DM) square adder. The DM square adder architecture is a combination of DML and DMADD techniques. By incorporating the DM square adder in processors, power dissipation can be reduced. The full adder used in dual-mode square adder is static energy recovery full (SERF) adder which is faster and consumes less power compared to conventional full adder. For Braun multiplier using DM square adder power consumption is reduced by 63.54% and speed is increased by 90%. The proposed designs are implemented using mentor graphics tools in 130 nm technology.

Keywords: dual mode logic; DML; dual mode addition; DMADD; DM square adder; SERF adder; Braun multiplier; low power.

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Biographical notes: B. Jaya Lakshmi did her MTech in VLSI Design in 2016 from the MVGRCE (A), JNTUK, Kakinada. She is currently working as an Assistant Professor in the Department of ECE, Lendi Institute of Engineering and Technology, Vizianagaram.

R. Ramana Reddy did his MTech (I&CS) in 2002 from the JNTUK, Kakinada, MBA from AU in 2007 and PhD in 2008 in Antennas from AUCE (A), AU. He is presently working as a Professor and HOD of ECE in JNTUA College of Engineering, Pulivendula, Kadapa. He published around 90 technical papers in journals and conferences. He is a senior member of IEEE, Fellow of IE, IETE, and member of ISTE and ISOI. His research interests include antennas, EMI/EMC, VLSI, and embedded systems.

Naresh K. Darimireddy obtained his BTech in ECE from the NBKRIST, ME in EC from the UVCE (A), Bangalore University, MBA from the Central University, Pondicherry, and PhD from the UCEK (A), JNTU, Kakinada. He has 15 years of industry and teaching experience. He is a

member of IEEE, IEEE A&P Society, and IE. He is qualified as a UGC-NET candidate in 2013 and has 35 technical publications in journals and conferences. His research interests include microwave antennas, filters, RF receivers and DRAs.

1 Introduction

A series of repeated additions is considered for the process of multiplication. Addition is the basic operation in performing multiplication, division and subtraction. Design of high speed and low power multiplier using different full adder circuits are proposed (Levi et al., 2014). The multiplier blocks are the key hardware blocks in many applications like digital communications, digital signal processing systems and FPGA's, etc.

The multiplication operation involves generating and accumulating the partial products. The shift and add algorithm multiplication adds X partial products together. Each partial product is generated by the AND gate and the partial products are added by full adders. If there is a carry, it is propagated to the next bit position. Various power reduction techniques using low threshold levels in implementing the four-bit multiplier with carry-select adder is proposed (Liao et al., 2002). High speed arithmetic circuits using a multiple valued current mode MOS integrated technique with booth encoded algorithm is proposed (Watts, 1989). Reversible logic is employed to design multiplexer-based full adders and multipliers (Landauer, 1961). The implementation of sum and carry operations are done by using multiplexer control input techniques and Shannon-based technique for designing high performance and low power multipliers (Senthilpari et al., 2008).

An optimised four-bit modified-gate diffusion input (MOD-GDI) technique is proposed for high speed and low power array multiplication (Kishore et al., 2017). Two different 16-bit multipliers are proposed with an approach of partial products of the multiplier are altered to introduce varying probability terms. With this method power savings up to 72% and 38% is achieved by the two variants (Venkatachalam and Ko, 2017).

16 bit optimised area efficient ripple carry adder (RCA) and carry look ahead (CLA) adders are reported based on the theory of reversible logic to attain theoretical zero power dissipation and high efficiency (Yadav and Khandelwal, 2017). Two different topologies of 12 different one-bit full adders to design four-bit full adders are proposed based on sub-threshold logic to achieve low power (Ghobadi et al., 2010). Carry skip and carry look-ahead BCD adders are designed using two transistors, AND gate with no power supply and OR gate with no ground to attain low power (Thapliyal et al., 2006). Wang and Sung (2009) presented low power Braun multiplier by using different threshold voltage techniques (Vasefi and Abid, 2005). By sacrificing transistor count, a full adder with 11 transistors is proposed for temperature sustainability and improved power consumption (Sinha et al., 2011). Using two-dimensional by-passing method, the power dissipation is minimised by more than 75% compared to prior proposed designs (Wang and Sung, 2009). A comparison between Braun and Wallace multiplier techniques is presented. A new shift and add method is proposed to attain high speed and low power dissipation (Sangeetha and Khan, 2018). Wallace tree-multiplier is implemented based on full swing gate diffusion input (GDI) logic and CLA adder (Mohan and Rangaswamy, 2016). With lowest MOS transistor count, a high-performance low-power 32-bit ripple-carry full adder is reported in Nehru and Shanmugam (2014).

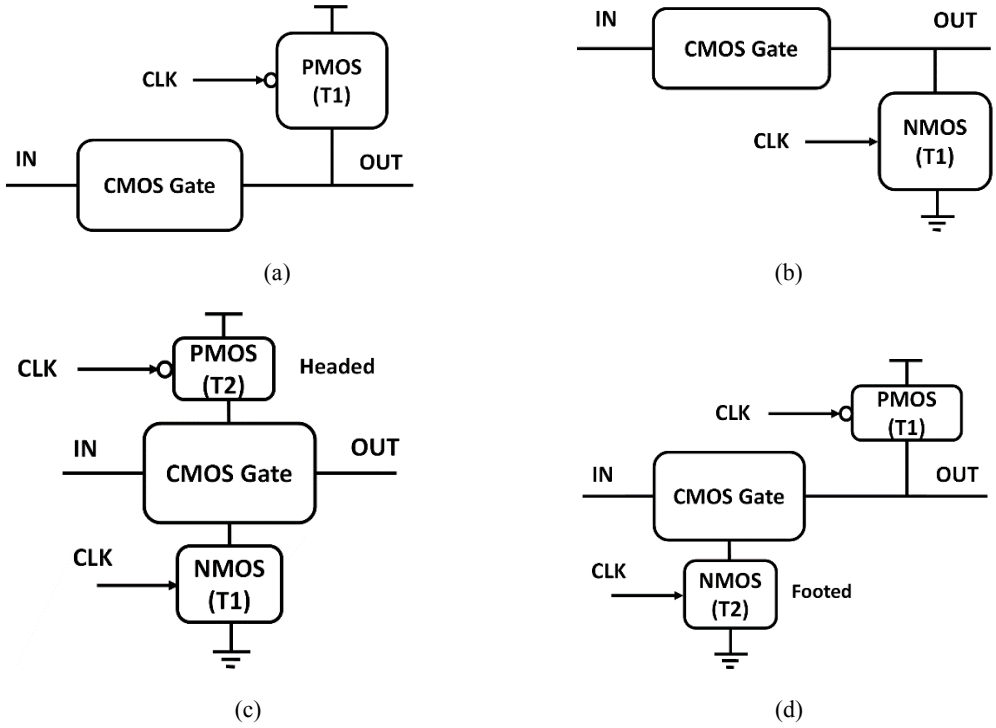
In this paper, a low power and high speed Braun multiplier is implemented using dual-mode (DM) square adder. Dual-mode square adder is a combination of DML and dual-mode addition (DMADD) techniques. The proposed design yields good performance and low power dissipation. Proposed designs are implemented using mentor graphics tools in 130 nm technology.

2 Dual mode logic

Dual mode logic (DML) gate is similar to static CMOS gate with an additional transistor. The gate of the additional transistor is connected to clock signal. DML gate is simple and sizing scheme of transistor is required to achieve desired performance. DML switches between two operating modes such as static and dynamic operating modes (Kaizerman et al., 2013; Levi et al., 2012, 2013; Levi and Fish, 2013). In static mode it consumes less power and works faster in dynamic mode. In static mode the clock transistor is always in off state, the output depends on the operation of standard CMOS gate. In dynamic mode the clock enables and works in two different modes, that is pre-charge and evaluation modes. The DML technique has four different topologies, i.e., type-A, type-B, headed and footed topologies. In type-A DML topology the PMOS transistor (T1) is connected at the output as shown in Figure 1(a). When the clock input is low the PMOS transistor (T1) conducts and the output is pre-charged to VDD. When high input clock signal is applied, the PMOS transistor (T1) is cut-off and the output depends on logic of the CMOS gate. In type-B DML topology the NMOS transistor is connected at the output with drain terminal to the ground as shown in Figure 1(b). When the clock input is low the NMOS transistor (T1) is cut-off and the output depends upon the logic of standard CMOS gate. When the clock input is high the NMOS transistor conducts and the output is pre-charged to ground, thus the DML is operated in both static mode and dynamic modes. Headed and footed topologies are presented in Figure 1(c) and Figure 1(d), respectively. The headed and footed topologies allow successful pre-charge

for a cascaded topology of standard static gates. A NAND gate is implemented using all four DML topologies to compare the performance of DML topologies. The schematics of NAND gate using DML topologies are shown in Figures 2(a)–2(d).

Figure 1 Various types dual-mode logic topologies: (a) type-A DML, (b) type-B DML, (c) headed DML and (d) footed DML



Comparison of NAND gate performance in different DML topologies is presented in Table 1.

Type-B DML topology consumes less power and achieves high speed compared to other DML topologies.

Table 1 Comparison of performance of NAND gate for all the four DML topologies

Parameters	*NAND gate*				
	Conventional design	*Type-A DML*	*Type-B DML*	*Headed DML*	*Footed DML*
Power (watts)	50 u	386.3 n	1.057 n	230.68 n	386.3 n
Delay (sec)	50.16 n	50.072 n	212.27 p	50.096 n	100 n

Figure 2 NAND gate schematic of DML topologies: (a) NAND gate schematic of type-A DML, (b) NAND gate schematic for type-B DML, (c) NAND gate schematic for headed DML and (d) NAND gate schematic for footed DML

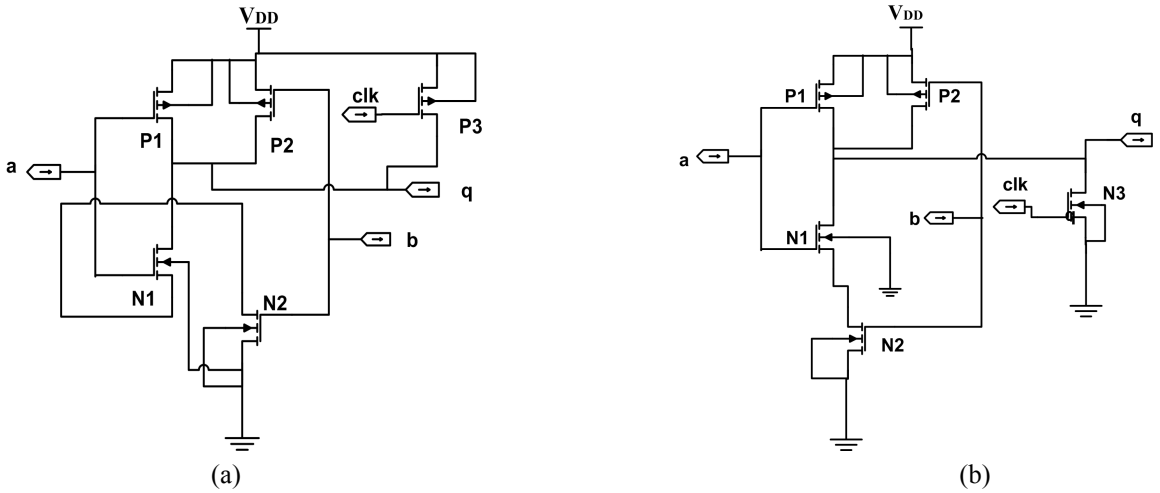
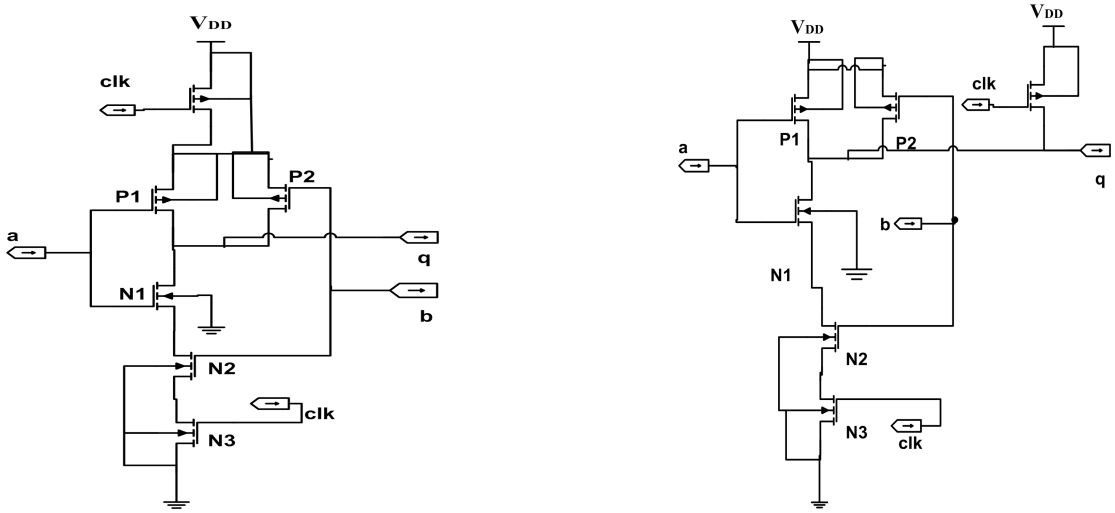


Figure 2 NAND gate schematic of DML topologies: (a) NAND gate schematic of type-A DML, (b) NAND gate schematic for type-B DML, (c) NAND gate schematic for headed DML and (d) NAND gate schematic for footed DML (continued)



(c) (d)

3 Conventional dual-mode addition

DMADD technique works in two modes (Wimer et al., 2014), normal addition mode and extended addition mode. In normal mode, the addition can be done in only one clock cycle by taking the advantage of carry probability. In extended modes, it sometimes requires more clock cycles to complete addition. Control circuit is required to decide whether to work in normal mode or in extended mode. When DMADD is used in pipelined processor the control circuit is used to select the proper mode at instruction decode stage.

For an n-bit adder, DMADD comprises m groups of k bits each, where n = m * k, so the propagation delay of carry meets the clock cycle for two bit adders. The voltage scaling, high threshold voltage and transistor downsizing for an n-bit DMADD enables (2k – 1) bit delay. If carry propagates more than (2k – 1) bits, m clock cycles are used to compensate the carry. The carry probability of m groups in normal mode is:

$$Q_{norm}(k, m) = (1-2^{-k})^{m} = 1 - m.2^{-k} + O(2^{-2k}) > 1 - m.2^{-k}$$

The probability in extended mode is:

$$Q_{ext}(k, m) < m.2^{-k}$$

In pipelined processor, the DMADD requires m cycles in extended mode. DMADD achieves low power dissipation but imposes performance degradation and design overhead. So DML is used to avoid the extended addition mode (multi cycle mode).

4 Implementation of DM square adder

The design and methodology of DM square adder architecture is a combination of DML and DMADD techniques. The control circuit and DM square adder is shown in Figure 3. For an n bit RCA, DM Square adder is divided into m = n/k groups of k bits each. The carry does not propagates more than (2k – 1) bits. The probability of carry is $m/2^k$ in extended mode through which it propagates 2k – 1 bits. By doing the unconventional sizing of the transistor in worst case the carry path for n bits must be completed in a given clock cycle.

The full adder used in DM square adder is static energy recovery full (SERF) adder, shown in Figure 4. The SERF adder achieves less delay and consumes low power compared to conventional full adder. The DML RCA in DM^2 adder topology is implemented using SERF type-B DML logic. At the sum node the adder achieves full output voltage due to presence of adder at the output node. SERF adder has no direct path to ground. Elimination of ground reduces the power consumption.

The SERF adder is implemented in all four topologies of DML and the results are tabulated in Table 2.

From the results, it is evident that the type-B DML SERF adder consumes low power and achieves less delay. The schematic diagram and layout of DM2 adder is presented in Figures 5 and 6, respectively.

Table 2 **SERF adder with DML topologies**

Parameters	*SERF adder*	*SERF adder with DML logic*			
		Type-A DML	*Type-B DML*	*Headed DML*	*Footed DML*
Power dissipation (watts)	6 n	94 u	3.2 n	6.6 n	96 u
Delay (sec)	116.1 p	49.54 n	49.52 n	49.54 n	49.54 n

Figure 3 The control circuit and dm square adder

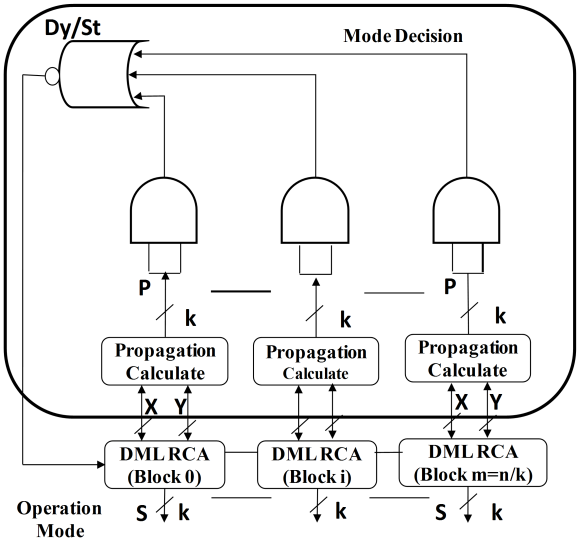


Figure 4 SERF adder

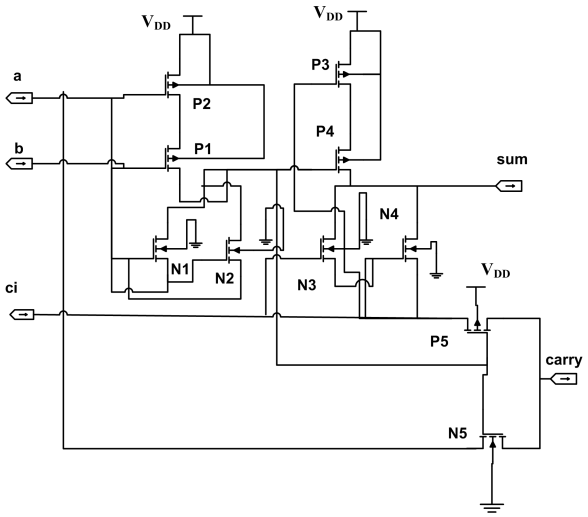


Figure 5 DM square adder schematic diagram (see online version for colours)

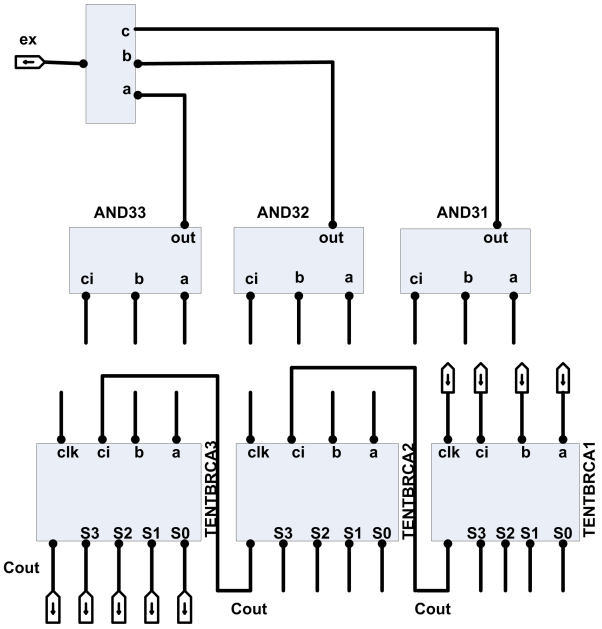
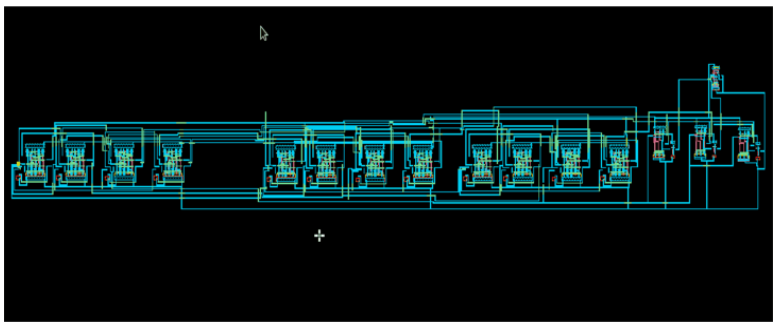


Figure 6 DM square adder layout (see online version for colours)

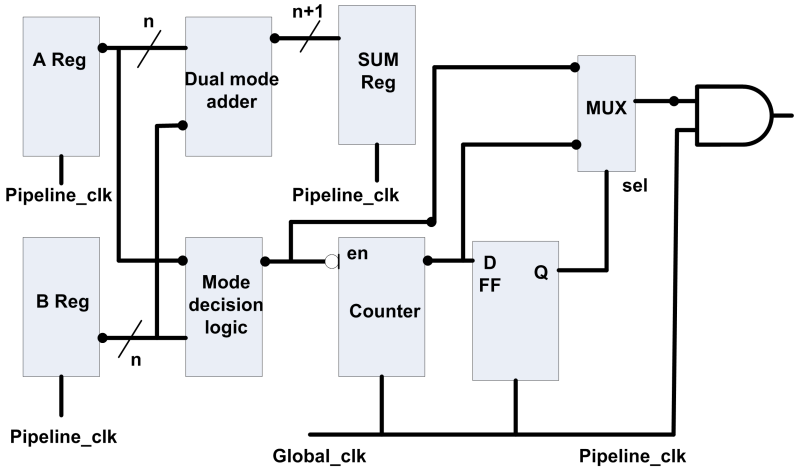


The type-B DML logic gives the best performance, by taking the advantages obtained from type-B DML topology. Different types of adders like one-bit full adder, four-bit RCA and DM^2 adder are implemented. Comparison of performance of designed adders in terms of power dissipation and delay are presented in Table 3. From the results DM^2 adder using SERF adder with DML consumes less power and achieves high speed. In distributed architecture and wireless electronics there is a need to design circuits that work at high speed. High throughput can be achieved by using pipelining technique. In a pipelined processor the DM Square adder targets the carry propagation of k bits, which requires only one cycle in normal mode and additional clock cycles to complete addition in extended mode.

Table 3 Comparison of different types of adders in different topologies

Type of adder	*Topology*	*Delay (sec)*	*Power (watts)*
Full adder (one bit)	Conventional design	199.1 p	6.1 m
	Conventional design with DML	50 n	1.5 m
	SERF adder	116.1 p	3.58 n
	SERF adder with DML	49.52 n	3.52 n
Ripple carry adder (four-bit)	Conventional design	50.62 n	78.5 m
	Conventional design with DML	99 n	3.1 m
	SERF adder	49.5 n	14.2 n
	SERF adder with DML	49.5 n	14 n
DM2 adder	Conventional design	57 n	192 m
	Conventional design with DML	28 n	9.98 m
	SERF adder	50.3 n	31 m
	SERF adder with DML	25.7 n	57 n

Figure 7 DM square adder embedded in pipelined processor (see online version for colours)



The DM square adder embedded in a pipelined system is shown in Figure 7 and its schematic is presented in Figure 8. The arguments are stored in reg A and reg B. When these arguments are stored in registers A and B, the reg SUM starts with addition SUM = A + B. The mode decision logic is used to select the normal mode or the extended mode. In

normal mode, the global clock is followed by pipeline clock; this pipeline clock is produced by clock gate. The sum is loaded in reg SUM after one clock cycle. In extended mode the pipeline clock is delayed by number of global clock cycles that makes the adder to complete addition operation. The extended mode occurs rarely but requires additional clock cycles. The extended mode can be handled by stopping the clock cycles of registers storing the operands. The simulation wave form of DM square adder embedded in pipelined system in which the output follows the input pipeline clock is shown in Figure 9. The mode decision can be done simultaneously with addition. The addition is done in normal mode when mode output is '1' and in extended mode when mode output is '0'.

Figure 8 Schematic diagram of DM square adder embedded in pipelined processor (see online version for colours)

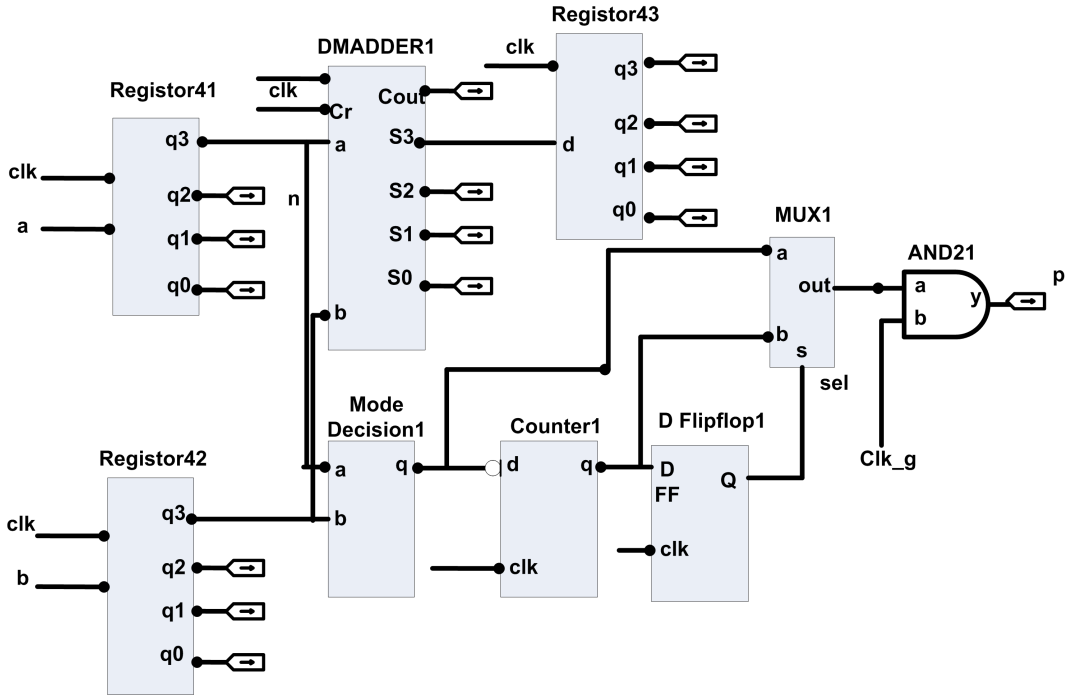
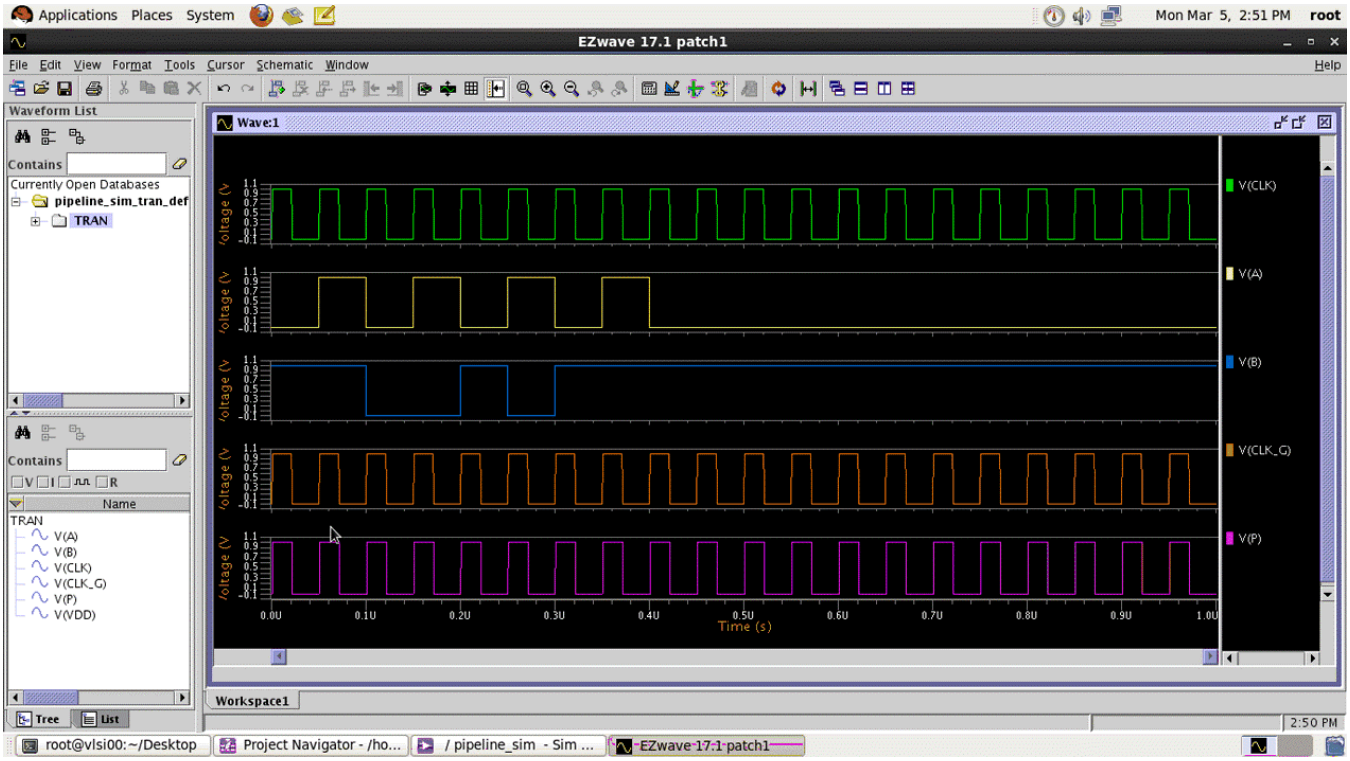


Figure 9 Simulation waveforms of DM square adder embedded in pipelined processor (see online version for colours)



5 Multiplier

Multiplication is done by using full adders. For an m bit adder it takes X clock cycles to compute multiplication operation (X is bit wide of A input and Y is bit wide of B input). The binary representation of multiplication is:

$$A = \sum A^i 2^i,\ i = 0 \text{ to } 4\ (X = 4)$$

$$B = \sum B^j 2^j,\ j = 0 \text{ to } 4\ (Y = 4)$$

$$A^i \text{ and } B^j \in (0, 1)$$

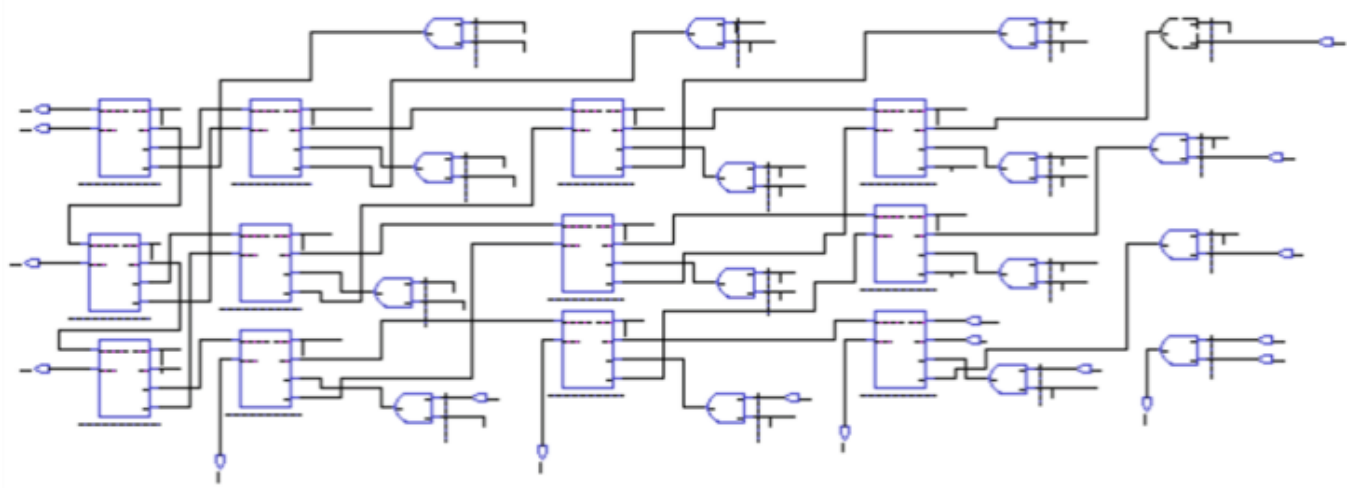
$$C = A * B = \sum C_k 2^k = k = 0 \text{ to } X + Y - 1$$

$$\left(\sum A^i 2^i,\ i = 0 \text{ to } X\right)\left(\sum B^j 2^j,\ j = 0 \text{ to } Y\right)$$

$$\sum\left(\sum A^i B^j 2^{i+j}\right),\ i = 0 \text{ to} X - 1,\ j = 0 \text{ to } Y - 1.$$

The DM square adder is used as the basic building block to implement the multiplier. In this paper Braun multiplier is implemented using DM square adder with SERF adder with DML. The schematic diagram of Braun multiplier using DM Square adder is presented in Figure 10. Braun multiplier is also known as the carry save array multiplier which is a parallel multiplier and as non-additive multiplier because it does not add additional operand. It consists of array of AND gates and full adders to perform multiplication. It performs the multiplication for the unsigned numbers.

Figure 10 Braun multiplier using DM square adder (see online version for colours)



For an n bit Braun multiplier n(n – 1) adders and n^2 AND gates are required. The product is generated by the AND gate by taking the X and Y inputs. By using the row of full adders the partial products can be added to sum of the previous partial products resulting in the final product output with carry. Input waveforms, output waveforms and layout of Braun multiplier are shown in Figures 11–13, respectively.

6 Results

DM square adder is a combination of DML and DMADD techniques. Different types of DML techniques are analysed and results are presented in Table 1. Performance of SERF adder with different DML topologies is compared in Table 2. Performance comparison of DM square adder in different topologies is tabulated in Table 3. Braun multiplier is implemented using conventional design, proposed SERF adder and proposed DM square adder. Results are compared with other designs reported and tabulated in Table 4. Delay of the proposed multiplier is less compared to other designs and the power consumption is also less expect (Kishore et al., 2017). All the designs are implemented using mentor graphics tools in 130 nm technology.

Table 4 Comparison of performance of proposed multiplier

Ref.	*Braun multiplier*	
	Power (watts)	*Delay (sec)*
Liao et al. (2002)	54.3 u	4.6.95 n
Kishore et al.	492 p	214 p
Vasefi and Abid	45.6 u	5.27 n
Wang and Sung	145.48 u	3.97 n
Conventional	81.4 n	49.96 n
Proposed SERF	176 n	127.2 p
Proposed DM^2	*63.10 n*	*12.2 p*

Figure 11 Braun multiplier input waveforms (see online version for colours)

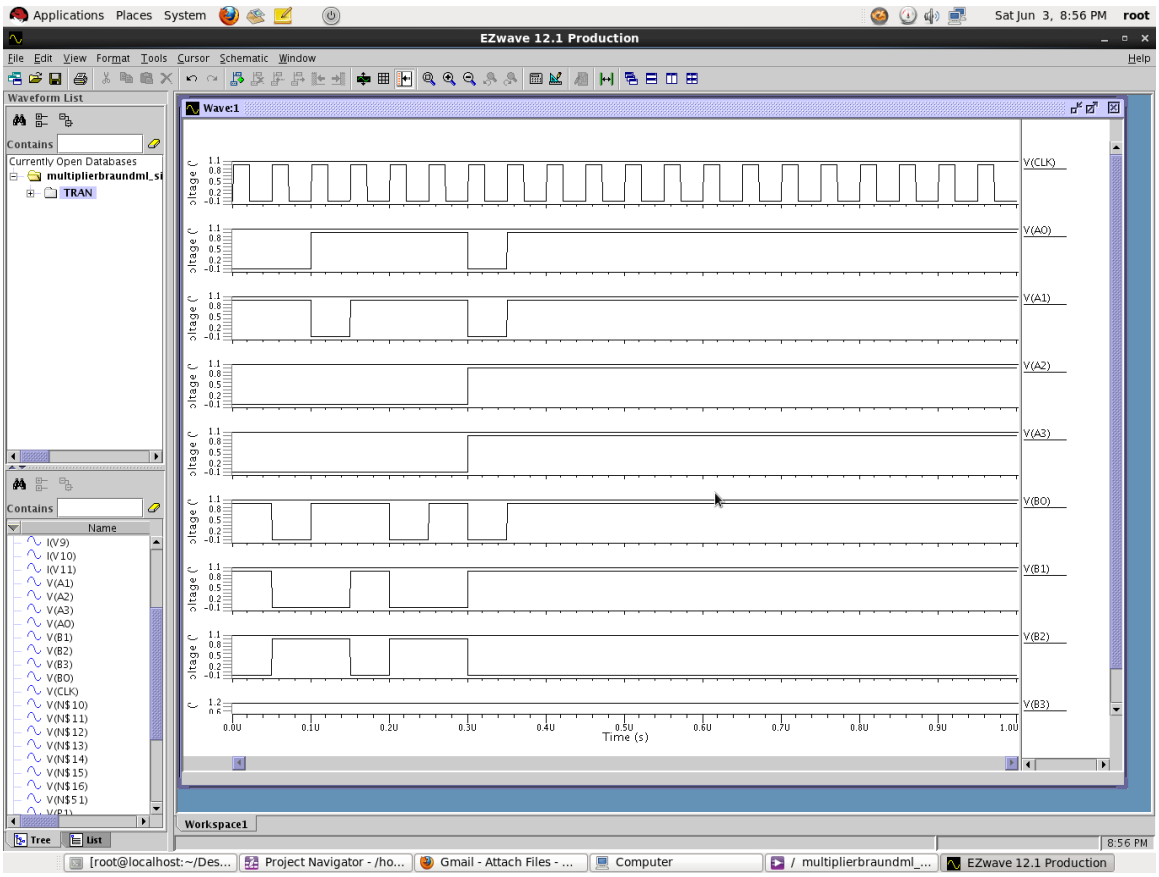


Figure 12 Braun multiplier output waveforms (see online version for colours)

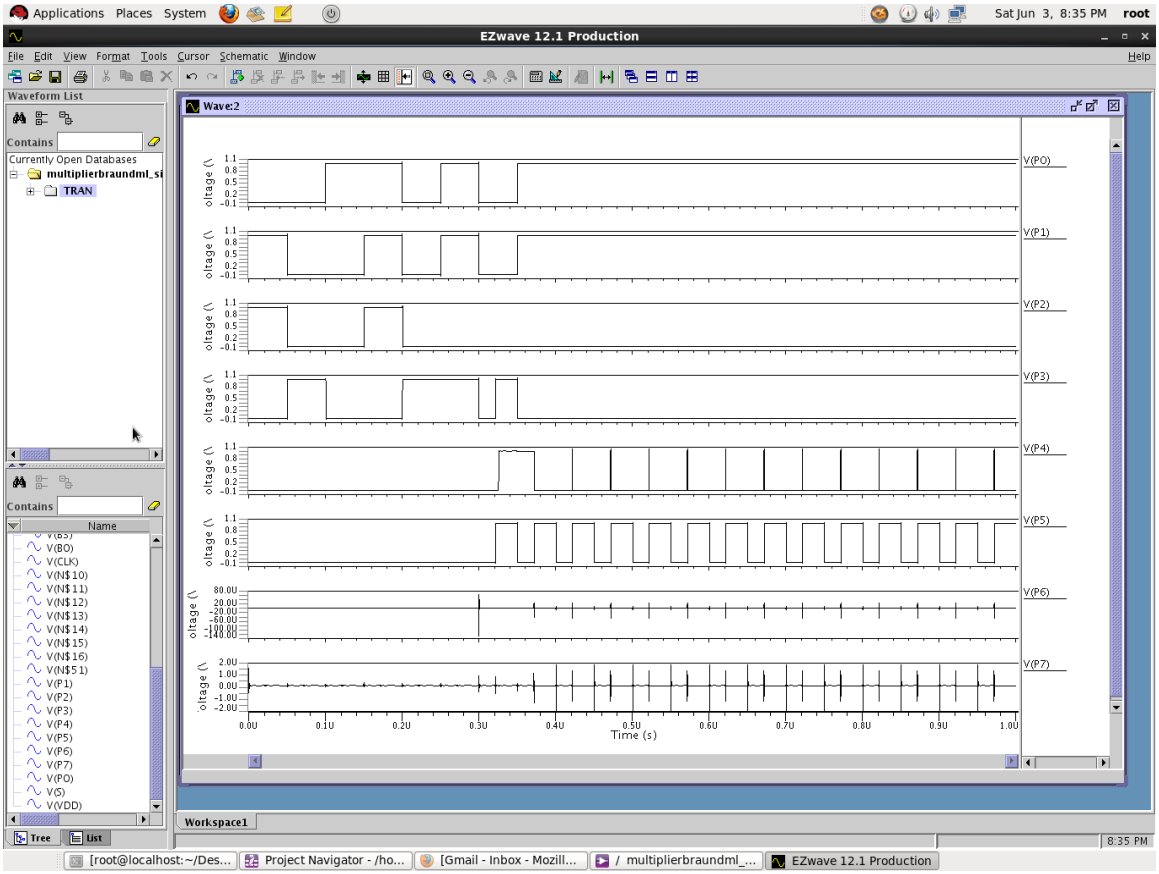
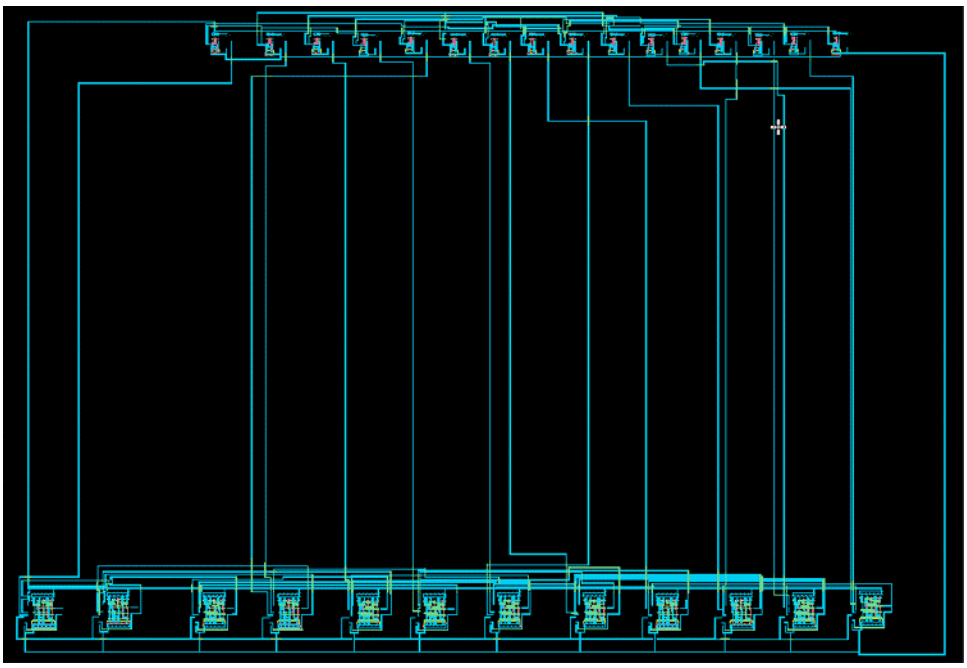


Figure 13 Braun multiplier layout (see online version for colours)



7 Conclusions

The low power and high speed multiplier is designed using DM square adder. The DM square adder is implemented using DML and dual mode addition. The full adder used in DM square adder is SERF adder. Braun multiplier is designed using the proposed DM square adder and its performance parameters are compared with different designs. For the proposed multiplier design power consumption is reduced by 63.54% and speed is increased by 90% compared to conventional designs.

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